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This report describes the development of a CMOS static memory capable of electronic read and write and parallel optical write. The memory is designed to receive optically transmitted data from a holographic read-only memory. A 16-bit memory was designed, fabricated, and tested using Argon and Helium-Neon lasers. Power levels for optically written data is approximately 3.4 micro Watts per pixel. Extensive applications are suggested.

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DESIGN OF INTEGRATED CMOS CIRCUITS FOR PARALLEL DETECTION AND STORAGE OF OPTICAL DATA

A THESIS
Presented to
The Academic Faculty

by

Andre Harding Sayles

In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in Electrical Engineering

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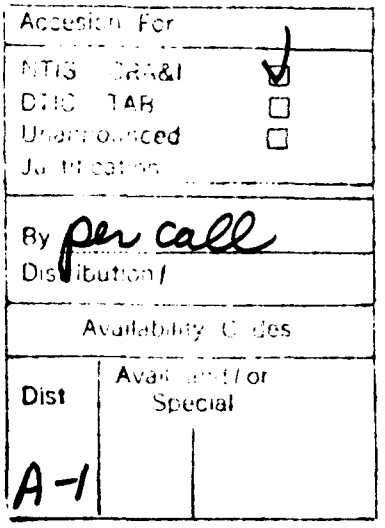
August 1990

DESIGN OF INTEGRATED CMOS CIRCUITS FOR PARALLEL DETECTION AND STORAGE OF OPTICAL DATA



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SUMMARY

A CMOS circuit capable of storing optically transmitted data from a holographic read-only memory (ROM) is described. The investigation focuses on combining optical and electronic circuit technology to rapidly transfer data in parallel fashion from a ROM to an array of static random-access memory (SRAM) cells. The proposed optoelectronic SRAM cells have an optical detection component as well as electrical read and write functions.

Development of the optoelectronic memory circuit is based on research in several areas. A design method is described which applies MOS inverter transfer characteristics to the six-transistor CMOS SRAM cell. Circuit diagrams, layouts, and models are presented for photodetection devices adapted to integrated CMOS circuits. These devices are fabricated in standard CMOS processes for silicon. Performance characteristics are provided for photodetection devices with different load circuits. The optical data transfer technology is extended to other systems in which high speed and parallelism are essential.

An array of the optoelectronic cells and many related devices and circuits have been designed, fabricated, and tested. Simulation and experimental results are given for circuits applicable to optical detection and electronic storage of data. The optical data transfer concept has been verified with a 16-bit optoelectronic SRAM. Data contained in a parallel array of 16 light beams with an average power of 3.35 μW per bit were successfully transferred to the SRAM. The Argon laser light pattern was formed by both a mask and a hologram. The storage of the optical information was verified by electrical addressing of each cell. This research is a fundamental component of a massively parallel optical-to-electronic data transfer system being developed. Data is to be transferred to a RAM from a page-oriented holographic ROM containing up to 10^{11} bits of volume-multiplexed data.

CHAPTER 1

INTRODUCTION

The unique properties of laser light are responsible for the rapid development of electro-optic technology over the past decade. Uniform spatial coherence, enhanced bandwidth, and lack of mutual interference are some of the vital attributes that make precisely controlled laser beams attractive for applications such as control of electronic circuits [1]. Despite anticipated near term advancements in electronic computer programming and architecture, the practical limitations of electrical interconnects and submicron technology will inevitably slow the evolution of electronic hardware [2, 3]. Because of these constraints, optical and optoelectronic processing [4] are likely to play a dominant role in computing technologies of the future.

One of the bottlenecks in many computing processes is the rate at which data stored in a large read-only memory (ROM) can be transferred to a random-access memory (RAM). The research presented in this thesis addresses that problem by proposing the use of electrical circuits for detection and storage of optically transmitted parallel data. This technology is termed an optical ROM-to-electronic RAM (ORER) data transfer system [5]. The goal is to develop and test static memory cells and propose other circuits capable of detecting and storing data contained in a parallel array of low power light beams. The data contained in the array of laser beams is assumed to originate from an optical ROM, which is a page-oriented holographic memory containing many bits of volume-multiplexed data [5]. An example of a complete optical ROM-to-electronic RAM data transfer system is

shown in Fig. 1-1. Two Bragg cells are shown as an example dual selection process for the holographic ROM. The first cell selects a specific volume, while the second cell selects a specific page within the chosen volume. Combining the hologram and selection process results in the application of a predetermined light pattern to the detector array within the RAM. The optical information is then stored as electrical data.

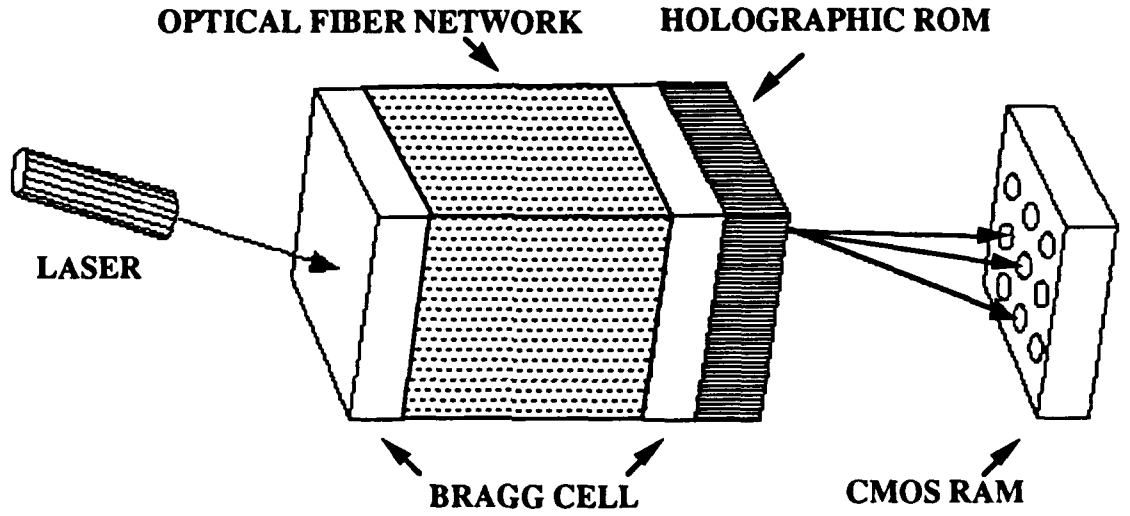


Figure 1-1. Optical ROM-to-Electronic RAM Data Transfer System. The first Bragg cell selects a specific volume. Within the designated volume, the second Bragg cell selects a wave front with a predetermined bit pattern.

1.1 Motivation

Much research has been completed on a number of automation-related topics, including massively parallel computer architectures [6-8], optical interconnection of VLSI systems [9], optical computing, and advanced artificial intelligence (AI) [10-12]. Optical computing has been successfully applied to a number of computationally intensive problems, such as equation solving [13] and digital logic [14]. The speed and parallelism inherent in optical computing have also made it attractive for artificial intelligence, which is one of the most computationally intense fields of computer science [15]. However,

progress in AI has been limited due to special requirements such as dynamic access to adequate data storage space.

Currently, MOS and bipolar technologies offer a wide variety of data storage devices for conventional electronic computers. Memories based on CMOS technology offer electrical flexibility, high packing densities, and data storage with extremely low power consumption. Progress in wafer technology and systematic improvements in integrated circuit fabrication processes have resulted in the realization of MOS devices with submicron channel lengths. Semiconductor memories using these smaller devices are complex and have very large capacities. Unfortunately, the future growth of such electronic memories is not without limits. The bit storage density, which approximately doubled every year during the 1970s, is now slowing as an apparent saturation point approaches. While memories were advancing in data storage capacity, corresponding progress was also shown in computer architecture. Currently, many areas of computing continue to advance via the field of optics. To keep pace with optical and parallel processors as well as the optical interconnect approach to communication problems [8], memories must be developed beyond the current electronic limitations. Thus, the purpose of the research in this thesis is to investigate a combined optical and electronic approach to parallel data storage.

1.2 Research Objectives

The principal research in this thesis combines optics and VLSI circuit technology to achieve parallel transfer of data from a holographic ROM to an electronic RAM. Applications for parallel data transfer as well as other CMOS circuits for processing and storage of optical data are also considered.

The main objective of this research is to develop a static random-access memory (SRAM) cell array capable of storing optically transmitted data in an optical ROM-to-electronic RAM data transfer system. The cells must also possess standard electrical read

and write functions. As part of the development of the SRAM cells for optical data transfer, several areas are studied. First, static RAM technology is investigated to determine the cell configuration most adaptable to photonic input. Photodetector technologies are also examined to find devices compatible with bulk CMOS fabrication processes. Other areas of investigation are VLSI circuit fabrication processes, SRAM cell design, stability, and operation, and applications for the optical ROM-to-electronic RAM technology. Applications are addressed in terms of optoelectronic circuits developed to meet the primary objectives as well as new circuits based on similar principles.

In the past decade holographic optical elements (HOEs) in free space have been applied to several areas of computing, including optical clock distribution and communication between circuits, chips, and wafers. For such applications, as well as the research presented here, the conversion of optical information to an electronic signal traverses many fields of electrical engineering. Those fields include laser optics, photonics, circuit theory, semiconductor device physics, and holography.

Other research involving free space HOEs has included special features such as gallium arsenide substrates [16]. However, in an effort to achieve short term results, the objectives of the research presented here are limited to circuits fabricated in a bulk CMOS process. Besides the known advantages of CMOS circuits, silicon technology is well established and offers low-cost fabrication through, for example, the MOS Implementation Service (MOSIS) [17].

Optoelectronic circuits are based on a combination of electronic theory and optics. Interfacing the two concepts is accomplished in this thesis by considering an SRAM cell to be a combination of simple digital CMOS integrated circuits. Simulation of the optical and electronic circuits also requires adaptation of one technology to the principles of the other. Thus, electronic models for photodetection devices are investigated for the purpose of

simulating the optical and electrical circuits at the same time. Simulations are generally conducted using the SPICE circuit simulator.

The final objective is to provide experimental support for the principal optoelectronic circuits as well as other fundamental circuits and devices necessary for verification of basic concepts. Experimentation in this thesis ranges from a simple photodetector device fabricated in a CMOS process to optoelectronic SRAM cells in a 16-bit array. Due to photodetector requirements, all circuits used in the experiments are fabricated in a p-well process.

1.3 Related Research

Although optical computing received serious attention as early as the 1970s [18] and has resulted in significant developments in the last decade, some numerical computing applications will not necessarily evolve directly from electronic systems to fully optical systems. For those applications, computers having both electronic and optical processes will serve as an intermediate step [19]. The most prevalent example of such a system is the optical interconnect technology introduced in 1984 as a potential means of relieving clock skew problems [20, 21] and reducing the required number of electrical input/output pins on a VLSI chip. Research on the applications of optical interconnections was quickly extended from the chip level to wafer-scale integration [22, 23]. Three general types of optical interconnects have been proposed: optical fibers [24]; integrated waveguides [16, 25]; and free-space connections via a holographic optical element [26, 27]. A general free-space optical interconnect system is composed of a light source, an HOE, and a network of photodetectors that are electrically connected to the VLSI circuit. The HOE is an off-chip device that defines the interconnection pattern and directs the light beams to a specific set of detectors. A variety of HOE types [28, 29] are available for addressing the detector network in an optical interconnect system.

Optical interconnect technology has been proposed as one of the many potential methods of implementing parallel architectures [30] necessary to meet the computational demands of artificial intelligence [10]. While much of the research associated with parallel computing and AI has focused on processors, interconnects, and input/output structures, only minor attention has been given to parallel memories. As a result, massively parallel optical-to-electronic data transfer was proposed in 1988 as a means of combining optics and electronics to achieve parallel access to an existing memory structure. Although many other principles are involved, the basic concept of using parallel optical beams to write to a static memory is derived from optical interconnect technology.

Much of the research presented in this thesis is based on a six-transistor CMOS static RAM cell. The full CMOS flip-flop circuit with cross-coupled inverters became a practical static memory cell in the 1970s. Since it contains only six transistors, the simple appearance of the cell conceals its actual complexity. In lieu of a concise design methodology for the CMOS SRAM cell, the literature has focused on stability and upset analyses [31-36], which have extended into the late 1980s. Approaches to prediction of static RAM cell upset have included phase-plane [37] and metastability [38] analyses.

While the CMOS static RAM technology is relatively new, photodetection devices required for converting optical energy into an electrical signal have been in existence for several decades. However, these have generally been discrete devices designed specifically for photon detection. Devices fabricated in a bulk CMOS process, such as needed for optical data transfer, have not been fully characterized. Numerous differences exist between conventional photodetectors and detectors that can be used in the optical-to-electronic data transfer technology. The most critical problem for the latter devices is the restricted junction depth imposed by the CMOS fabrication process. Some measurements of the response of these detectors [39] have been reported as part of optical interconnect research.

In other related research, optical interconnect technology has been applied to a static RAM in an attempt to speed up conventional addressing of individual memory cells. In large RAMs, much of the delay can be attributed to highly resistive and capacitive address lines. Although this research is not concerned with parallel access, it does apply an optical circuit directly to the word line of a static RAM cell. This optical addressing technique proposed by Wu *et al.* [40] provides both electrical and optical selection of individual word lines. A separate select switch is provided for the optical addressing circuit. When the optical addressing network is inactive, a tri-state inverter isolates the photodetection circuits from other components of the RAM. Additional work on optical data storage includes a conceptual optical memory as a component of a hybrid optical computing system [19] and a theoretical parallel memory based on interconnected optical logic devices [41].

1.4 Thesis Overview

This thesis contains seven chapters which examine techniques for the electronic storage of optical data. The fundamental storage element is a CMOS static RAM cell which has been modified for optical input. Complete optoelectronic data storage systems as well as individual components of such circuits are discussed. A simple, but explicit approach to CMOS SRAM cell design is presented. Photodetector devices compatible with CMOS circuits are then described. Detector load circuits are analyzed and then coupled with the detectors and the static RAM cell to form optical detection and storage circuits. Finally, applications for optoelectronic circuits are proposed. A brief outline of each chapter is provided below.

Chapter 2 starts with a discussion of the components and operation of a full-CMOS SRAM cell. In the remainder of the chapter, several design parameters that normally apply to single or cascaded inverters are presented in the context of the cross-coupled inverters making up a static RAM cell. A noise margin is extracted from the parameters and

compared to the static noise margin derived specifically for a six-transistor cell. The more explicit approach to design given in this chapter is relevant to cell modifications addressed in Chapter 5.

Chapter 3 examines photodetector devices applicable to bulk CMOS fabrication processes. The material in this chapter is applied to simulation of optoelectronic circuits in later chapters. The discussion centers around a basic pn junction detection device, which is formed during the drain implant for p-channel MOSFETS. After a review of the photodetection process, models for SPICE simulations are proposed. Simulations are used to compare the different models.

The next chapter introduces basic circuits for conversion of photons to an electrical voltage or current. Since the circuits in Chapter 4 are the basis of a static RAM cell, they are kept as simple as possible. Several optoelectronic configurations which offer a variety of advantages and disadvantages are illustrated. Simulations are provided for all circuits. Experimental results are also provided for selected circuits which have been fabricated and tested. Most of the circuits in this chapter are designed to be connected directly to a static RAM cell as discussed in Chapter 5.

Chapter 5, which contains the central work of the thesis, details the design and analysis of optoelectronic SRAM cells. The discussion includes both simulation and experimental results for several circuits, which have been proposed for electronic storage of optical data. Since the circuits described in this chapter are fundamental to the research, the results are significant to the continuation of work in this area.

Chapter 6 lays the foundation for additional research by investigating potential applications and suggesting other optoelectronic circuit configurations. The final chapter summarizes the research presented in the thesis and outlines the results and conclusions.

CHAPTER 2

DESIGN AND ANALYSIS OF CMOS SRAM CELLS

This chapter details the design and analysis of a CMOS-based SRAM memory cell which can be modified to detect and store optical data. Other optoelectronic storage devices and circuits are addressed in Chapter 6. As shown in Fig. 2-1, the CMOS SRAM cell is a flip-flop circuit composed of four MOSFETS which form two cross-coupled inverters. Two additional MOS transistors are used for access. Each access device is controlled by a word line and connected as a pass transistor from a bit line to an inverter input/output node. The two inverter outputs also serve as the data storage nodes of the cell. Although the cell is somewhat simple in appearance, the design and analysis of the flip-flop circuit have been the subject of extensive research. In lieu of analyzing the circuit by addressing dynamic properties of the inverters in the metastable region [38, 42], a less complex graphical approach to design is presented in this chapter. The results are supported by static noise margin (SNM) [35] calculations.

2.1 CMOS SRAM Cell Electrical Operations

The electrical operation of the cell is explained by simple read and write functions. Reading and writing of data refers to information stored at the DATA node (D), while the complementary information is automatically stored at the NOT DATA node ($\overline{D}$). Information is written to the cell when the word line (WL) is raised to a logic one while the BIT line and NOT BIT line (BL and $\overline{BL}$) are set to the desired pattern. A logic one, for example, may be written when $\overline{BL}$ is low and BL is either high or floating. When both bit lines and WL are high, the stored data remains unchanged. Reading the cell is similar to

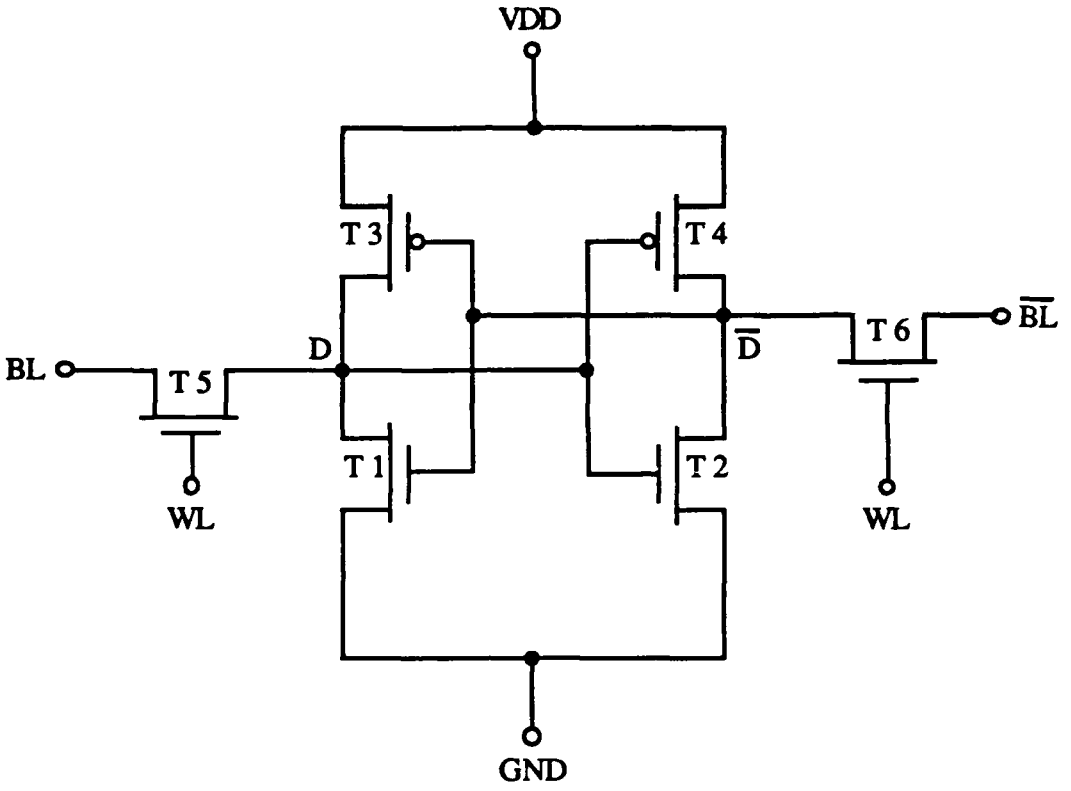


Figure 2-1. Standard Six Transistor CMOS SRAM Cell.

to the write operation, except the bit lines are precharged and then floated to allow transfer of data from the cell to the bit lines.

When the cells are arranged in a matrix to form a static RAM, individual cells are addressed by row and column decoders. The RAM also includes read/write control gates, buffered input/output buses, and sense amplifiers which detect and hold the state of the BIT and NOT BIT lines. The primary advantage of a static RAM is that the stored data is held without the need for refreshing. On the other hand, the RAM requires a large chip area which slows the time required for addressing individual cells [43, 44]. Access times for electrical read/write functions range from hundreds of nanoseconds for large conventional memories to less than 15 nanoseconds for circuits having minimum

geometries and advanced addressing techniques [45-48]. Static RAM circuits may also be designed for either clocked or non-clocked operation [49].

2.2 CMOS SRAM Cell Design

Recently, significant attention has been given to the study of stability in CMOS flip-flop circuits [37-38, 50]. Specific areas of interest are metastable operation [38] and static noise margin [35]. Metastable operation primarily focuses on the CMOS flip-flop during a change of states, although it also applies to the destruction of stored data. Static noise is any DC disturbance such as a series voltage or parallel current at the input of one of the cross-coupled inverters. Noise may also be in the form of a voltage at the ground line or power supply, or any combination of the these sources.

The objectives of a stability analysis are to obtain the proper operation of a static RAM cell during transition and ensure the ability to retain stored data indefinitely. The temporary loss of data is called a soft error when the cell continues to function properly after the upset event. Soft errors are often caused by ionizing radiation. Loss of data may also be the result of noise from a variety of sources, or a change in state during a read operation. The design process developed in this chapter is based on the retention of data during the worst-case read operation; however, improved stability in one area generally results in less susceptibility to other sources of error as well. The parameters discussed in the next sections are normally used in the design of simple inverters made up of n-channel (NMOS) and p-channel (PMOS) transistors. However, after the basic design parameters are discussed, it will be shown that they can also be conditionally applied to cross-coupled inverters and, thus, the CMOS SRAM cell. This explicit approach to CMOS static RAM cell design is essential to the design of optoelectronic circuits presented in Chapters 4 and 5. More complex design and analysis methods presented in references cannot be readily extended to static RAM cells which are modified for optical input.

2.2.1 Inverter Threshold

A voltage transfer curve for a CMOS inverter is shown in Fig. 2-2. The threshold voltage (V_{th}) of the inverter is the voltage level at which the output voltage equals the input voltage during a switching event. It is considered the transition point for the output voltage of a single inverter as well as the cross-coupled inverters of the CMOS RAM cell.

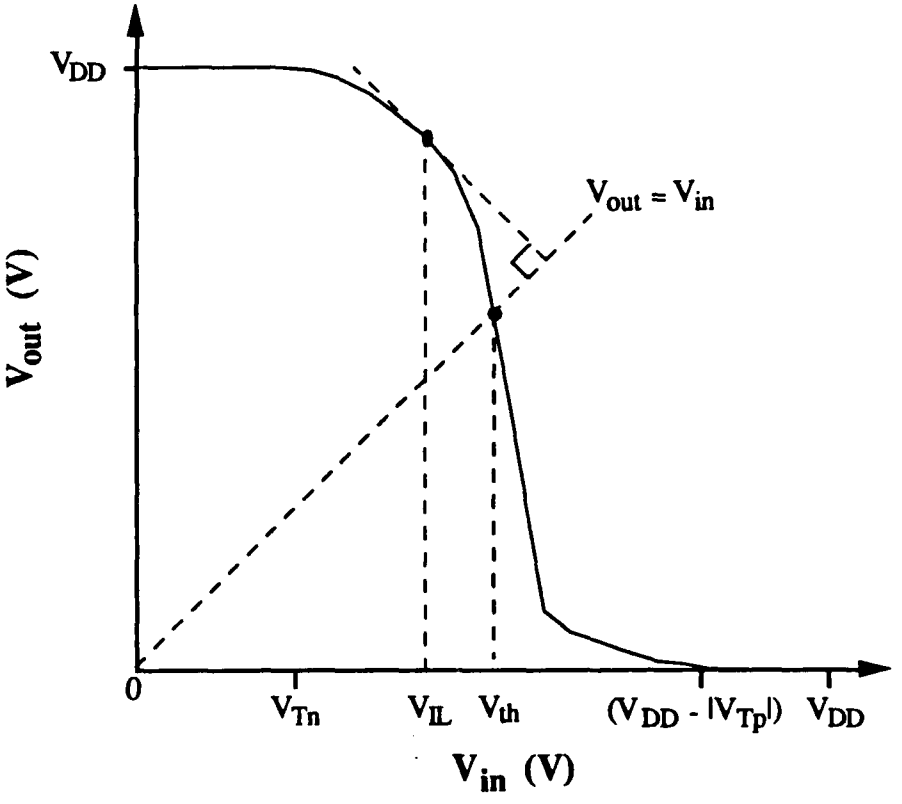


Figure 2-2. Generalized Voltage Transfer Curve for a CMOS Inverter.

For a CMOS inverter, both the NMOS and PMOS devices are in the saturation region of operation when the output is at V_{th}. The maximum current flows through the devices at this point. By making the output voltage the same as the input voltage and equating the

saturation n-channel and p-channel transistor currents, the inverter threshold is [51]

$$V_{th} = \frac{V_{Tn} + \sqrt{\frac{\beta_p}{\beta_n}}\left(V_{DD} - |V_{Tp}|\right)}{1 + \sqrt{\frac{\beta_p}{\beta_n}}}, \tag{2.1}$$

where V_{Tn} and V_{Tp} are the n-channel and p-channel transistor threshold voltages, $ß_n$ and $ß_p$ are the respective transconductance parameters, and V_{DD} is the supply voltage. Using the device parameters and supply voltage given in Table 2-1, the CMOS inverter threshold is plotted in Fig. 2-3 as a function of PMOS transistor aspect ratio $(W/L)_p$ with the size of the NMOS device $(W/L)_n$ as a parameter. The graph shows the inverter threshold increasing with NMOS transistor channel length, but inversely proportional to PMOS device channel length. Generally, for static RAM cell design the inverter threshold need not be set midway between the power supply rails (0 and 5 volts). In fact, if other factors are disregarded, a higher threshold will improve the operation of the cell since data is stored by writing a logic

Table 2-1. Numerical Values for Calculation of CMOS Inverter Threshold.

PARAMETER	UNITS	VALUE
V_{DD}	V	5.00
V_{Tn}	V	1.00
V_{Tp}	V	-0.74
k'_n	A/V^2	55.10E-6
k'_p	A/V^2	21.80E-6

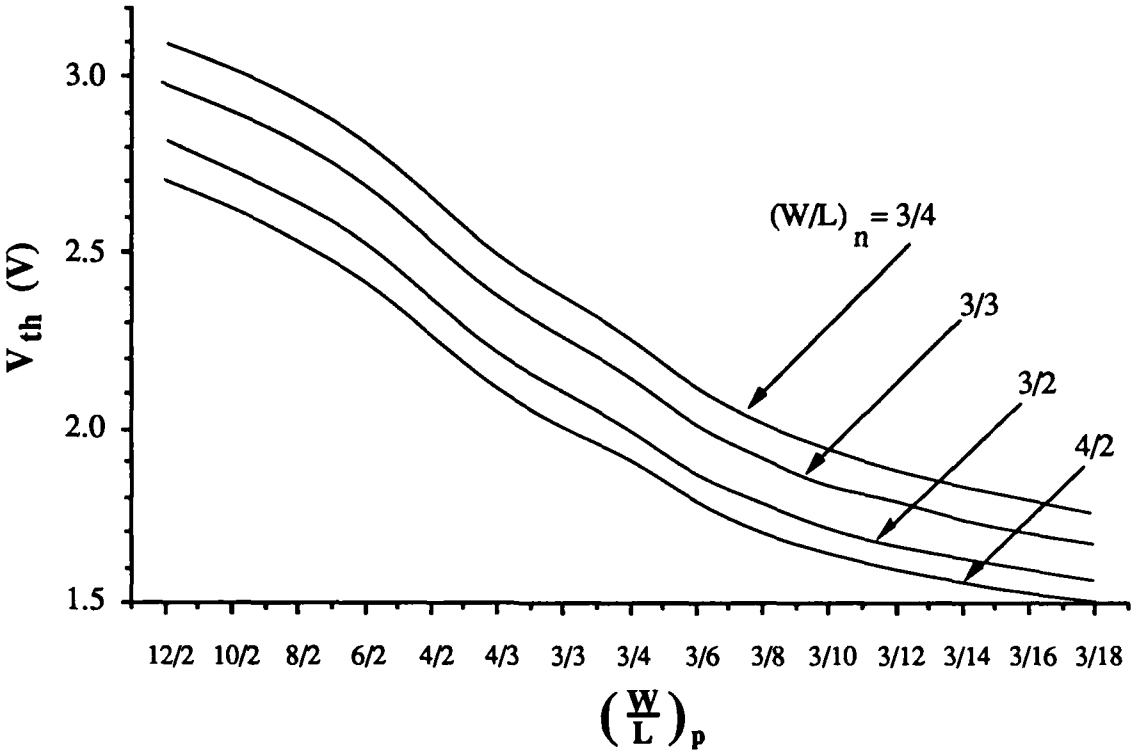


Figure 2-3. Threshold Voltage of a CMOS Inverter. Data are provided for selected PMOS transistor aspect ratios with the size of the NMOS transistor as a parameter.

zero to one side of the cell. However, it will become apparent in later sections that the size of individual transistors cannot be arbitrarily changed simply to increase or decrease the inverter threshold. Other aspects of circuit performance will be affected as well.

2.2.2 Inverter Input Low Voltage

The input low voltage V_{IL} is the maximum logic zero input to an inverter that assures a logic one at the output. Setting the current of the nonsaturated p-channel transistor equal to the current of the saturated n-channel device gives [51]

$$\frac{\beta_n (V_{IL} - V_{Tn})^2}{\beta_p (V_{DD} - V_{out})} = 2(V_{DD} - V_{IL} - |V_{Tp}|) - (V_{DD} - V_{out}) \qquad (2.2)$$

where V_{out} is the inverter output voltage. A second expression is found from the definition of V_{IL} shown in Fig. 2-2 as the point where

$$\frac{dV_{out}}{dV_{in}} = -1 \tag{2.3}$$

is satisfied. This gives

$$V_{IL}\left(1+\frac{\beta_n}{\beta_p}\right) = 2V_{out} + \frac{\beta_n}{\beta_p}V_{Tn} - V_{DD} - \left|V_{Tp}\right|. \tag{2.4}$$

Simultaneously solving equations (2.2) and (2.4) gives the inverter input low voltage as plotted in Fig. 2-4 for selected NMOS and PMOS transistor aspect ratios. Model parameters for the n-channel and p-channel devices are found in Table 2-1. The curves are similar to the plot of inverter threshold in Fig. 2-3. The value of V_{IL} increases when $(W/L)_p$ increases or when $(W/L)_n$ decreases. Inspection of Fig. 2-2 shows that a increasing V_{IL} assures a logic one output for a larger range of values for the inverter input voltage. Thus, when V_{IL} increases, a larger noise voltage is required to upset the cross-coupled inverters of a CMOS static RAM cell. The disturbance to a static RAM cell caused by reading a logic zero may be treated as a noise source for analysis purposes [35]. The relation of these parameters to the noise analysis is further explained in the next sections.

2.2.3 Inverter Output Low Voltage

In addition to the input low voltage described in Section 2.2.2, an inverter may be characterized by its output low voltage V_{OL}. The value of V_{OL} for the cross-coupled CMOS inverters in a six-transistor static RAM cell is approximately zero and not crucial to

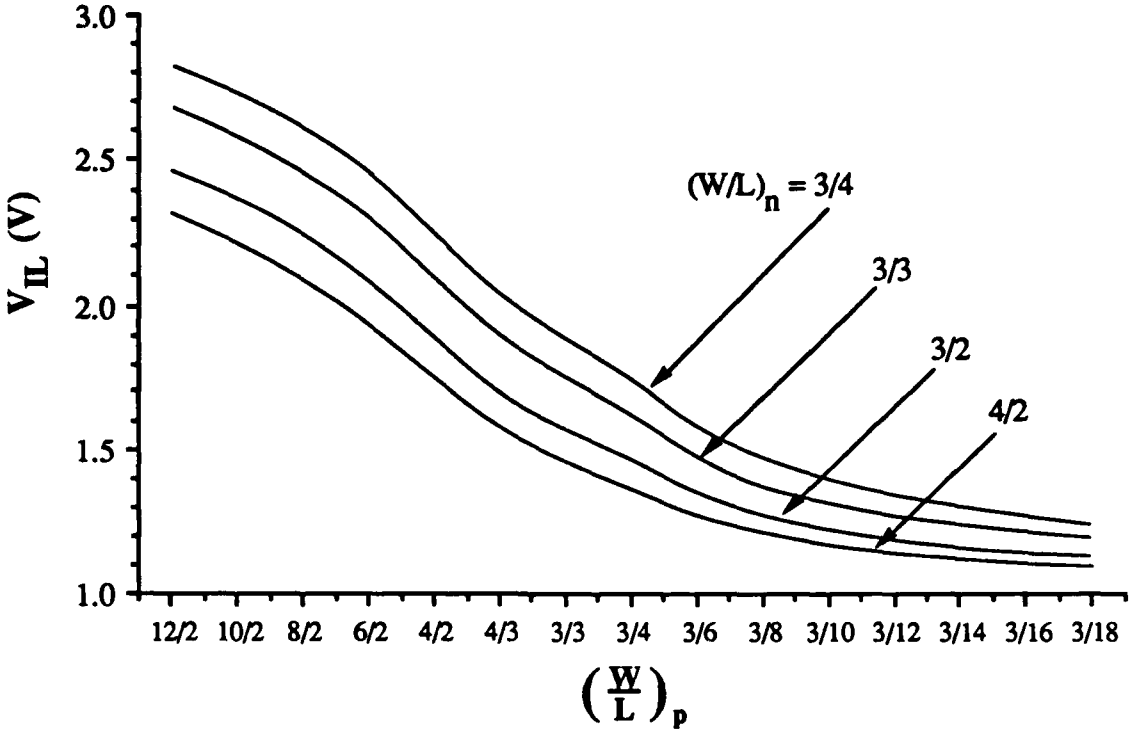


Figure 2-4. Input Low Voltage of a CMOS Inverter. Data are plotted for selected PMOS transistor aspect ratios with the NMOS transistor aspect ratio as a parameter.

the operation of the cell. However, during a read access event, two n-channel transistors form an inverter that is critical to cell stability. To read a logic zero from the DATA node of the cell in Fig. 2-1, the bit lines are first precharged. For purposes of this analysis, BL and $\overline{BL}$ are assumed to be precharged to the supply voltage level to establish the worst-case conditions. When the word line is activated, access transistor T5 becomes the saturated enhancement mode load of an inverter formed with NMOS transistor T1, as shown more explicitly in Fig. 2-5. The output low voltage of this access inverter must be small enough to ensure the stored data does not change from a logic zero state to a logic one. Disregarding all other sources of RAM cell upset, the DATA node will remain unchanged during a read access event if V_{OL} for the access inverter is less than the value of V_{IL} for the cross-coupled CMOS inverters.

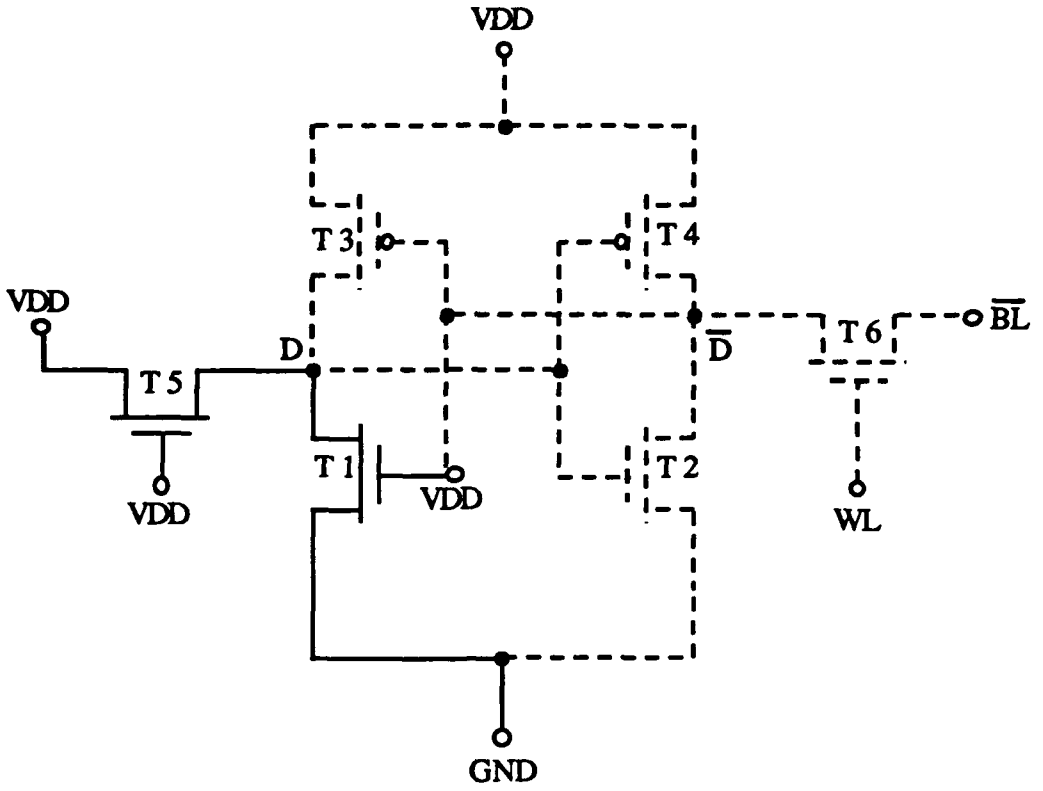


Figure 2-5. CMOS SRAM Cell Read Access Inverter.

The output low voltage of an MOS inverter with an enhancement-mode load is determined by setting the load transistor current equal to the driver current. The BIT line is set equal to the supply rail for the duration of this analysis. Degrading effects of the BIT line pull-up and the eventual BIT line discharge toward a logic zero are ignored. All NMOS devices in the SRAM cell are assumed to be fabricated simultaneously and, thus, have the same process transconductance parameter k'_n. When the access inverter load and driver currents are equal, the relationship between aspect ratios is given by

$$\left(\frac{W}{L}\right)_a = \left(\frac{W}{L}\right)_n \left[\frac{2(V_{DD} - V_{Tn})V_{OL} - V_{OL}^2}{[V_{DD} - V_{OL} - V_{Ta}(V_{OL})]^2}\right], \tag{2.5}$$

where the "a" subscript refers to the access transistor. To obtain equation (2.5), the NOT DATA node and, thus, the gate of T1 have been set equal to the supply rail. The threshold voltage is written as $V_{Ta}(V_{OL})$ since it is a function of V_{OL}. It includes body bias effects and must be calculated for each iteration in solving equation (2.5). Values for V_{OL} are plotted in Fig. 2-6 for selected access and NMOS transistor aspect ratios as shown. A smaller V_{OL} provides for a larger noise margin and a more stable RAM cell during a read access event. Inspection of Fig. 2-6 reveals that the value of V_{OL} decreases when $(W/L)_a$ decreases or when $(W/L)_n$ increases. However, the channel length of the access transistor cannot be increased without limit since the speed of the write operation and cell dimensions are also affected. Similarly, the size of the inverter NMOS transistor may not be increased

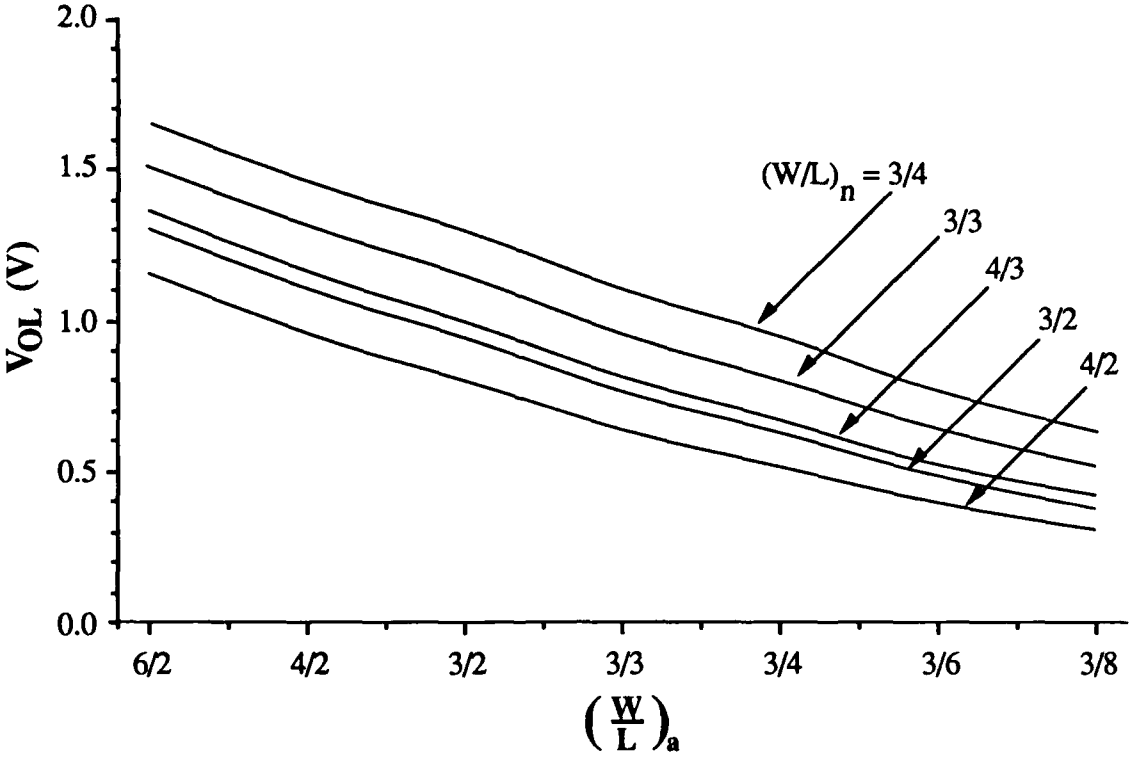


Figure 2-6. Output Low Voltage of Access Inverter. Data are provided for selected access transistor aspect ratios with $(W/L)_n$ as a parameter.

without affecting other cell design parameters. For example, a larger $(W/L)_n$ has a negative effect on V_{th} and V_{IL} as discussed in the previous two sections.

2.3 CMOS SRAM Cell Stability

A potential problem in static RAM cells is temporary loss of data or an upset event. Such loss of data can occur under static or dynamic conditions and may be caused by ionizing radiation [31, 52] or a variety of other events such as internal currents and threshold voltage shifts [34]. The likelihood of a soft error or loss of data is reduced by including a noise margin as part of the SRAM cell design. A CMOS static RAM cell is most susceptible to an upset event during the initial stage of an electrical read operation. In particular, transferring a logic zero to a precharged BIT line must not cause the state of the DATA node to change to a logic one.

In this section, two approaches to calculating the noise margin are presented. The first approach is to extract the low noise margin from the inverter parameters discussed in Section 2.2. Those results are then compared to the second noise margin which is a published method for calculating the static noise margin (SNM). Both analyses are based on cell stability criteria during a logic zero read operation.

2.3.1 Low Noise Margin

The noise margin for the CMOS SRAM cell is defined as the minimum noise voltage that will cause a logic zero level to exceed the input low voltage of the cross-coupled inverters. Thus, based on the inverter design parameters, the low noise margin is written as $NML = V_{IL} - V_{OL}$, where the input and output low voltages have been previously defined. Values for the noise margin are plotted in Fig. 2-7 for different size access and PMOS transistors when $(W/L)_n$ is equal to 4/2. Figure 2-8 shows the NML when $(W/L)_n$ is equal to 3/2. Only positive values of noise margin are shown in the graphs.

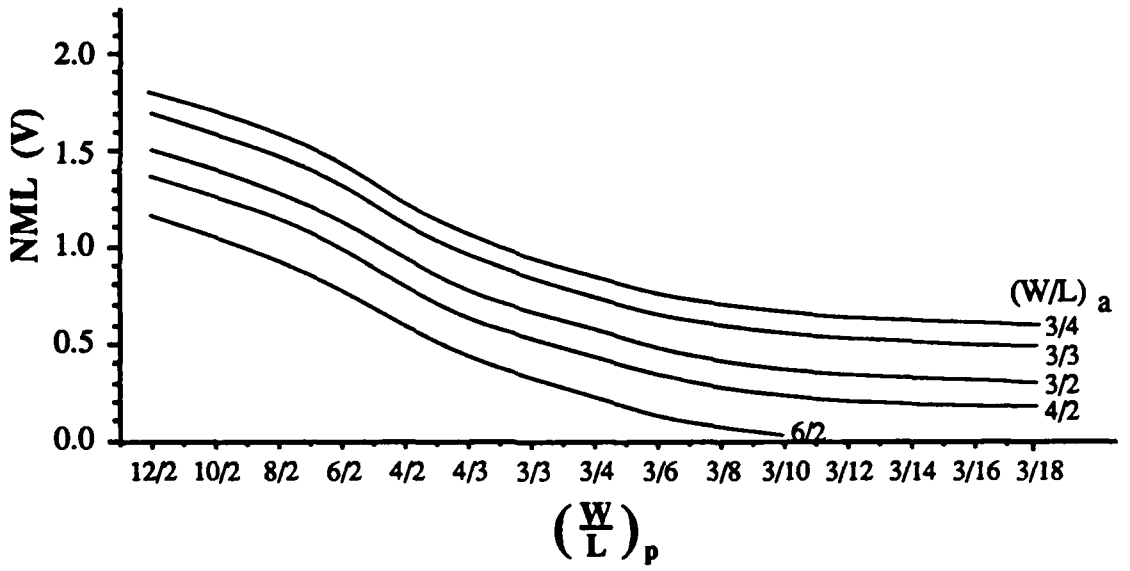


Figure 2-7. CMOS Static RAM Cell Low Noise Margin. Data are for selected PMOS transistor sizes with access transistor aspect ratio as a parameter and $(W/L)_n$= 4/2.

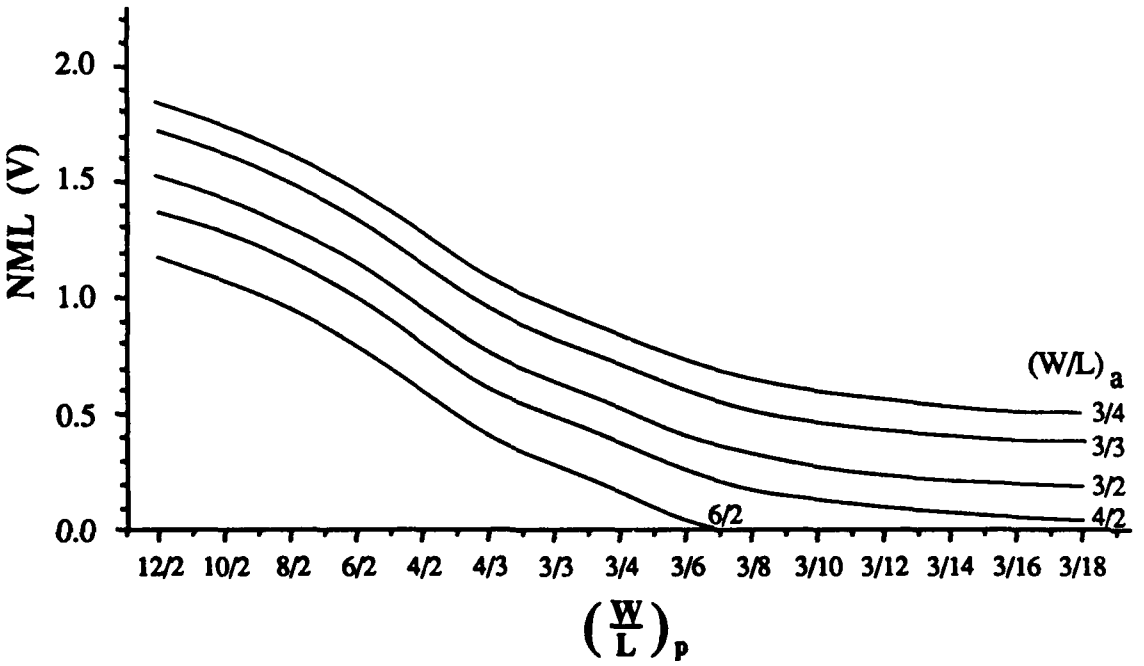


Figure 2-8. CMOS Static RAM Cell Low Noise Margin. Data are for selected PMOS transistor sizes with access transistor aspect ratio as a parameter and $(W/L)_n$= 3/2.

The values chosen for access, PMOS, and NMOS transistor aspect ratios must yield a positive value for the noise margin. A larger noise margin implies improved stability during the read cycle of the RAM cell. The required margin depends on the application of the SRAM cell. Since both V_{IL} and V_{OL} depend on the size of the NMOS transistor, a new set of NML curves is required for each value of $(W/L)_n$. The results shown in Figs. 2-7 and 2-8 reveal the actual trends in cell stability when the channel length of any of the six transistors is changed. The figures show an improved noise margin when $(W/L)_a$ decreases or when $(W/L)_p$ increases. Although both V_{IL} and V_{OL} increase when $(W/L)_n$ decreases, a comparison of the two graphs shows a net decrease in noise margin. This may be further explained by a larger change in output low voltage than input low voltage for a given change in $(W/L)_n$.

2.3.2 Static Noise Margin of a CMOS SRAM Cell

The second approach to noise analysis is the analytical measure of cell stability based on a complete CMOS SRAM cell discussed in this section. Seevinck *et al.* [35] derived explicit equations for the static noise margin of a six-transistor static RAM cell using basic MOSFET models. By neglecting second-order effects and linearizing the inverter transfer characteristics about an operating point, a fourth-order representation of the noise voltage was reduced to a second order expression. The equations could then be solved by application of the double-root stability criterion. The validity of this analytical model is supported by computer simulations of both the logic zero read-access mode and the data-retention mode in which the access transistors are held in cutoff by a low word line. The major shortcoming of the analytical model is that the n-channel and p-channel device threshold voltages are assumed to be of the same magnitude. Results of the static noise margin (SNM) analysis will be compared with the NML analysis described in the previous section.

Like the low noise margin, the SNM must be a positive number for cell stability during read access. Since it is based on a complete CMOS static RAM cell, the SNM is not useful for the design of optoelectronic SRAM cells discussed in a later chapter. The SNM is presented here primarily for verification of the NML calculations in Section 2.3.1. Where appropriate, the low noise margin based on inverter parameters will then be used for design of optical applications in Chapter 5.

The static noise margin is given in [35] as

$$SNM = V_T - \left(\frac{1}{k+1}\right)\left\{\frac{V_{DD} - \frac{2r+1}{r+1}V_T}{1+\frac{r}{k(r+1)}} - \frac{V_{DD}-2V_T}{1+\frac{kr}{q}+\sqrt{\frac{r}{q}\left(1+2k+\frac{r}{q}k^2\right)}}\right\} \qquad (2.6)$$

where $V_T = V_{Tn} = |V_{Tp}|$. Parameters introduced in equation (2.6) are defined in Table 2-2. The two most important parameters are $r = \beta_n/\beta_a$ and $q = \beta_p/\beta_a$. For a maximum SNM,

Table 2-2. Definitions of SNM Parameters.

SNM PARAMETERS
$r = \frac{\beta_n}{\beta_a}$ $\qquad$ $q = \frac{\beta_p}{\beta_a}$
$V_s = V_{DD} - V_T$ $\qquad$ $V_r = V_s - \left(\frac{r}{r+1}\right)V_T$
$k = \left(\frac{r}{r+1}\right)\left[\sqrt{\frac{r+1}{r+1-\left(\frac{V_s}{V_r}\right)^2}} - 1\right]$

both r and q must be as large as possible. This agrees with previous arguments since a larger NMOS device reduces the V_{OL} of the read-access inverter and a larger PMOS transistor increases the inverter V_{IL}. It can be shown that the SNM decreases when device threshold voltages decrease or when temperature increases. The SNM may be utilized as a measure of stability for an existing circuit, or as a tool for SRAM cell iterative design.

Since the published expression for static noise margin is based on a single threshold voltage, an error is introduced when $V_{Tn} \neq |V_{Tp}|$. As shown in Table A-1, the fabrication process used here does not satisfy this condition. A difference of approximately 0.25 volts is typical. Thus, a new expression for static noise margin has been derived for a CMOS SRAM cell in which $V_{Tn} \neq |V_{Tp}|$. The analysis gives:

$$SNM = V_{Tn} - \frac{1}{k+1}\left[\frac{V_{DD} - \frac{2r+1}{r+1}V_{Tn}}{1+\frac{r}{k(r+1)}} - \frac{V_{DD} - V_{Tn} - |V_{Tp}|}{1+\frac{kr}{q}+\sqrt{\frac{r}{q}\left(1+2k+\frac{r}{q}k^2\right)}}\right], \quad (2.7)$$

where the voltages in Table 2-2 are redefined as

$$V_s = V_{DD} - V_{Tn} \quad (2.8)$$

and

$$V_r = V_s - \left(\frac{r}{r+1}\right)V_{Tn}. \quad (2.9)$$

The static noise margin is plotted in Fig. 2-9 for $(W/L)_n = 4/2$ and the same access and PMOS transistor aspect ratios in Fig. 2-7. Values shown for the SNM are similar to those given in Fig. 2-7 for the low noise margin. For comparison, the SNM and NML curves for $(W/L)_a = 3/4$ are plotted on the same axis in Fig. 2-10. The plot shows that the

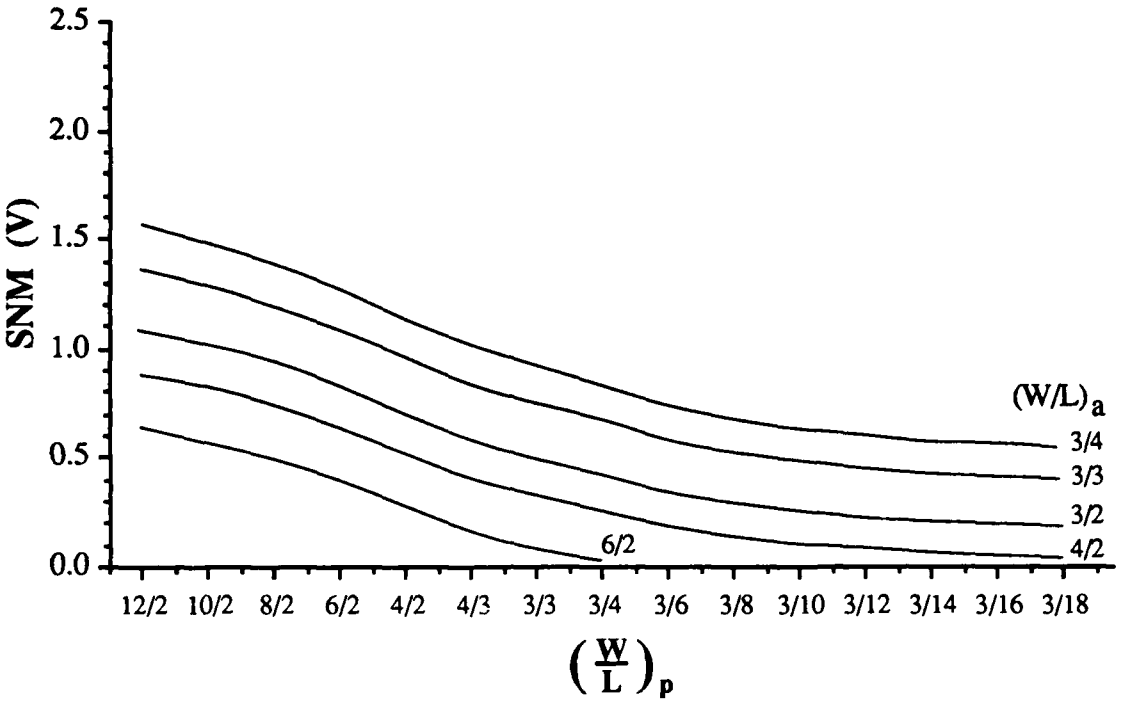


Figure 2-9. Static Noise Margin for a CMOS SRAM Cell. Data are for selected PMOS transistor sizes with access transistor aspect ratio as a parameter and $(W/L)_n$= 4/2.

NML is slightly larger than the SNM. However, when $(W/L)_p<1$, the SNM and NML are nearly the same. Results similar to those in Fig. 2-10 also hold for other combinations of access and NMOS transistor sizes. Thus, for a particular range of PMOS transistors, the NML is adequately close to the static noise margin to be useful for design of CMOS static RAM cells.

2.4 CMOS SRAM Cell Simulation Results

The operation of a simple six-transistor SRAM cell was verified using the SPICE circuit simulator. The model parameters listed in Table A-1 were extracted from three fabrication runs and averaged for use in the simulations. Aspect ratios for the respective transistors were chosen as $(W/L)_a = (W/L)_p$ =3/4 and $(W/L)_n$ = 4/2. Figure 2-11 illustrates the read and write operation of the cell. The value of V_{OL} for the access inverter is labeled

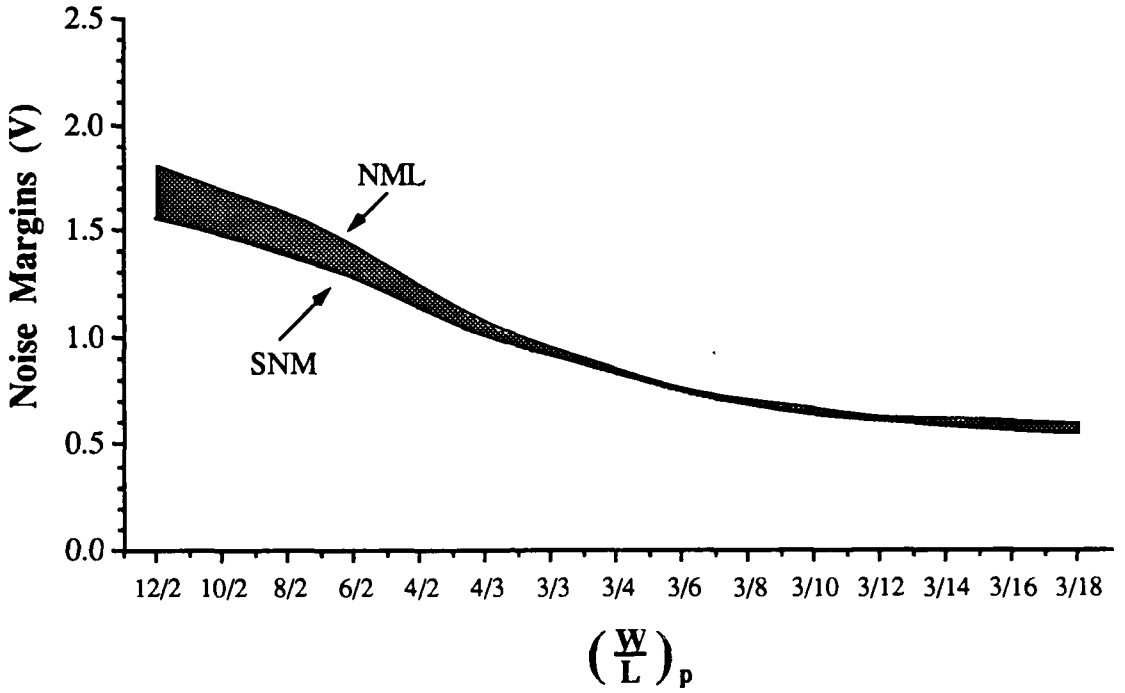


Figure 2-10. Comparison of CMOS SRAM Cell Static and Low Noise Margins. Data are for $(W/L)_a$= 3/4 and $(W/L)_n$= 4/2.

as READ ZERO. When this voltage is excessive, a soft error may occur. The transition of the DATA and NOT DATA nodes is shown in Fig. 2-12. Since these nodes correspond to the cross-coupled inverter inputs and outputs, the inverter threshold may be extracted from the graph. The value of V_{th} is not significantly changed by cross-coupling. Finally, the inverter V_{IL} may be extracted from the voltage transfer curve of Fig. 2-13. Simulations with and without cross-coupling gave the same results for V_{IL}.

Numerical values for design parameters and the NML have been extracted from the simulation results in Figs. 2-11 through 2-13 and listed in Table 2-3 for comparison with the predicted values and the SNM. All numbers pertain to the specific SRAM cell described at the beginning of this section. Examination of the table reveals a favorable

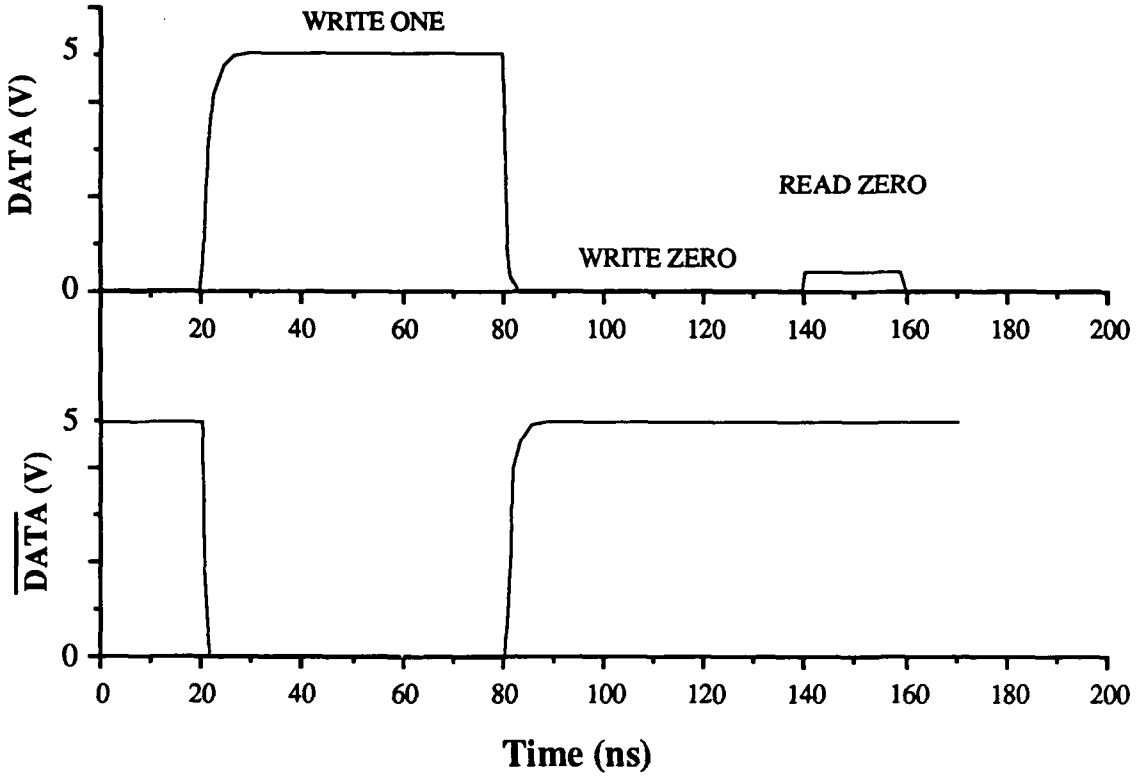


Figure 2-11. Timing Diagram for a CMOS SRAM Cell.

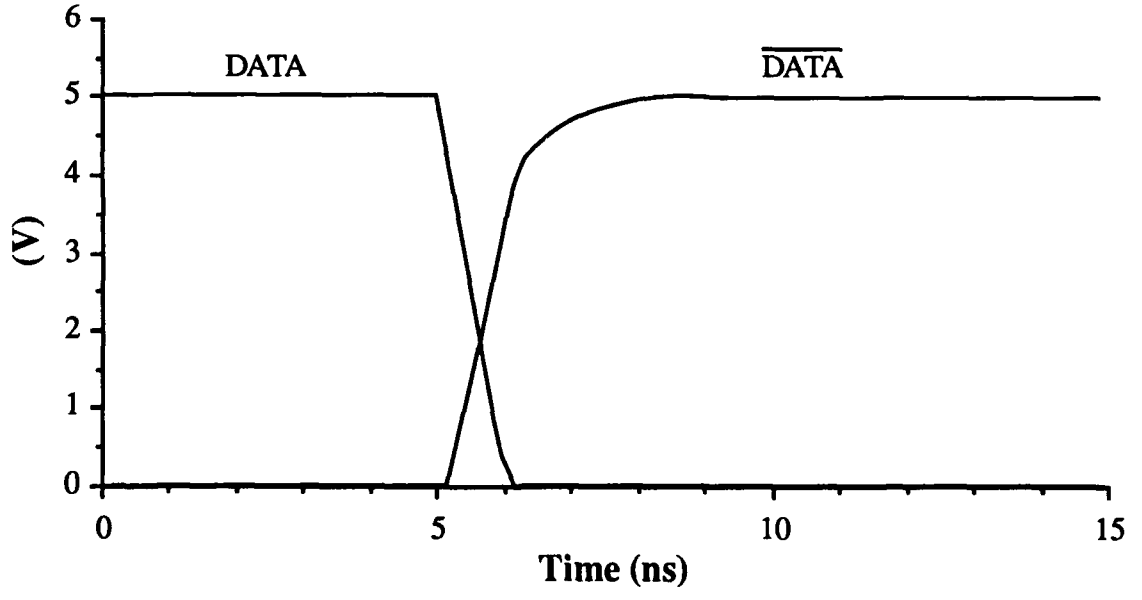


Figure 2-12. Transition of CMOS SRAM Cell Data Storage Nodes.

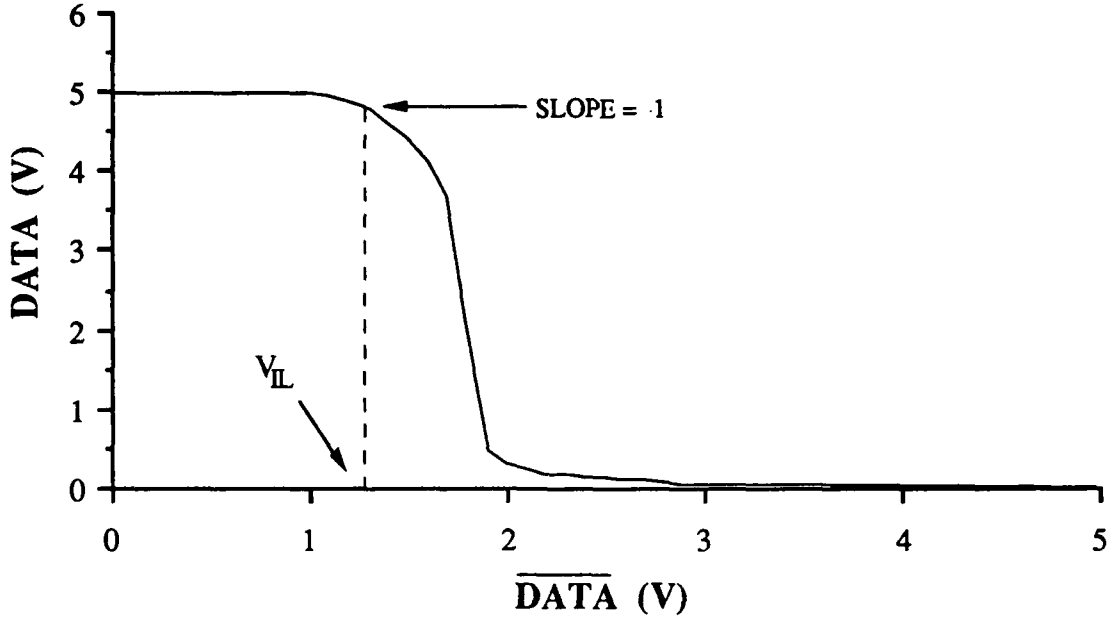


Figure 2-13. Voltage Transfer Curve for a Full-CMOS SRAM Cell.

Table 2-3. Full-CMOS SRAM Cell Simulation Results.

PARAMETER	CALCULATED	SPICE
V_{OL}	0.51	0.45
V_{IL}	1.37	1.31
V_{th}	1.91	1.88
NML	0.86	0.86
SNM	0.84	—

comparison between the theoretical and the simulation results. The simulations also support the similarity between the SNM and the NML when $(W/L)_p<1$.

In summary, several design parameters for single and cascaded CMOS inverters have been applied to cross-coupled inverters. A static noise margin has been derived for CMOS SRAM cells and used to verify the inverter parameter approach to cell design and analysis.

The low noise margin, which is extracted from the input and output low voltages, has been shown to be valid for a specific range of PMOS transistor aspect ratios. Although the individual parameters may be used for the standard six-transistor cell, they also apply to SRAM cells modified to store optical data. The optoelectronic SRAM cells are discussed later in this thesis. Since photodetectors are fundamental to electronic storage of optical data, modeling of those devices will be discussed in the next chapter.

CHAPTER 3

PHOTODETECTORS FOR CMOS INTEGRATED CIRCUITS

Photodetectors encompass a wide variety of devices, including pn junction diodes and phototransistors [53]. This chapter examines silicon photodetection devices that may be fabricated in bulk CMOS processes without additional fabrication steps. Since the devices are for specific optoelectronic applications, only pn junction diodes and phototransistors which are compatible with standard p-well processes are considered. Photoconductors are ignored because these devices generally have a slow transient response, as well as high laser power requirements [23].

Discrete devices designed specifically for photodetection are available in many different configurations and offer a wide range of performance characteristics. A type of detector can be selected based on general requirements and then fabricated to meet special conditions. Unlike discrete devices, the photodetectors discussed in this chapter must be derived from an existing fabrication process. Consequently, very little design flexibility is possible. For the optoelectronic applications presented in this thesis, the most serious limitations of these detectors are restricted junction depths and narrow depletion layers.

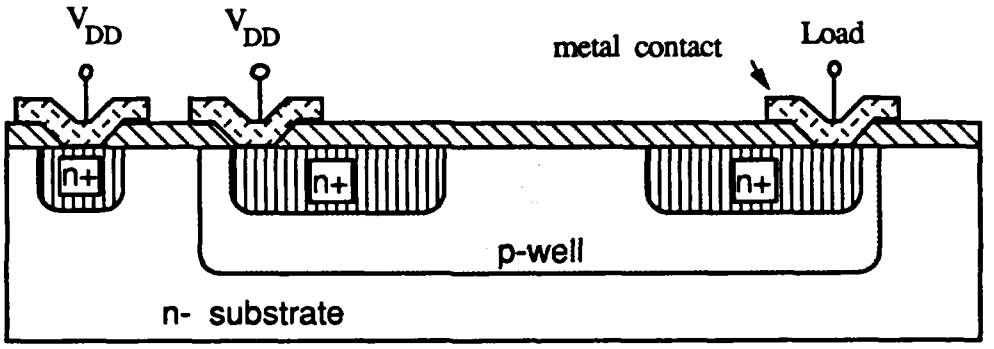
Several photodetector configurations that can be fabricated in a CMOS integrated circuit are described in the next section of this chapter. The discussion then concentrates on the detection process for a simple pn junction diode. The remainder of the chapter addresses performance and model requirements, and proposes two models for a pn junction photodiode. These models allow the simultaneous simulation of photodetectors and electronic circuits using the SPICE circuit simulator.

3.1 Detector Configurations

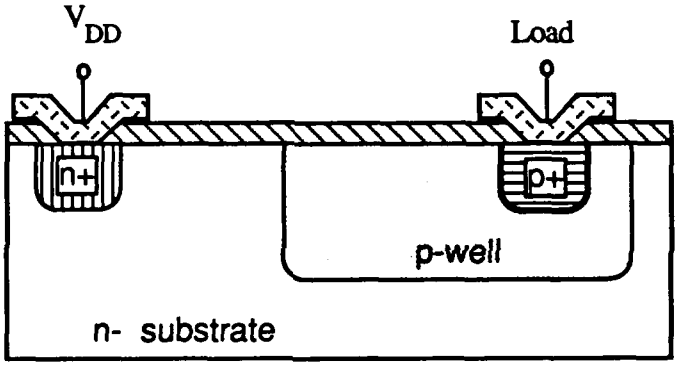
The purpose of this section is to describe four photodetector device configurations that may be fabricated in a bulk CMOS p-well process. Similar devices with the p and n regions reversed apply to n-well processes. A discussion of the fabrication steps and special characteristics is provided for each device. The vertical pn junction diode will be presented last, since it is the basis for the discussion in the remainder of the chapter.

Figure 3-1 shows a cross-sectional view of three photodetection devices that may be fabricated along with CMOS circuits. The lateral npn phototransistor in Fig. 3-1(a) is similar to an n-channel MOSFET without a polysilicon gate. An n^+ implant forms the transistor collector and emitter at the same time as the n-channel device drain and source during fabrication. Although the p-well base contact is omitted, one of the pn junctions will be forward biased during the detection process. Light absorption in the depleted base region creates electron-hole pairs and biases the transistor into the active region. When used as a photodetector, the npn transistor has a slower transient response time than a photodiode; however, the device also offers significant current gain [54]. Reduction of the base width increases the current gain of the transistor, but reduces the light sensitive area of the device. A larger photocurrent with a lower current gain is favored since the base-collector capacitance charging time tends to be the limiting performance factor in phototransistors [23].

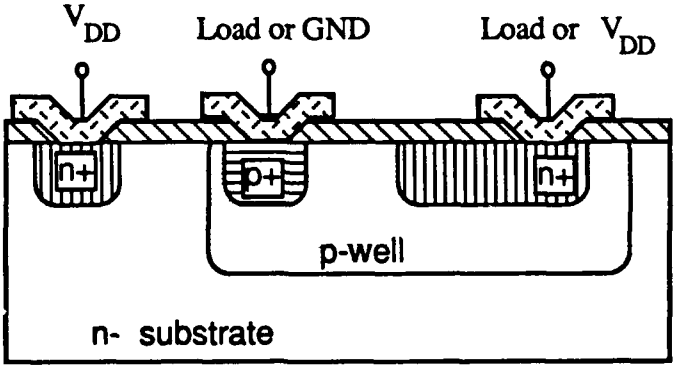
The photodetector in Fig. 3-1(b) has four distinct regions when the contact implants are considered. It is termed a lateral diode since the most efficient photon absorption occurs in the section of the depletion layer between the contacts for the p-well and the substrate. The photocurrent thus flows laterally to the p-well contact. The device has a good transient response and low parasitic capacitance, both of which are due to the relatively large depletion layer caused by the lightly doped substrate and p-well. Since



(a)



(b)



(c)

Figure 3-1. Photodetectors for a Bulk CMOS Fabrication Process. (a) Lateral npn phototransistor. (b) Lateral pn photodiode. (c) Vertical npn phototransistor.

most of the photocurrent originates in less than one-third of the depletion layer, the ratio of effective detector area to device area is poor.

An n^+ implant is added to the lateral diode to obtain the vertical npn transistor in Fig. 3-1(c). Although the base is too wide for this device to be a high current gain transistor, it works very well as a photodiode. When both n^+ regions are connected to V_{DD}, the device is a photocurrent source for a load connected to the p^+ implant ohmic contact. This configuration is a bipolar transistor with the collector-emitter voltage set to zero. With the p-well contact connected to ground, the detector is a photocurrent sink for a load connected to the n^+ implant inside the well. For the latter configuration, the incident light must be oriented to generate most of the electron-hole pairs in the depletion layer associated with the n^+ implant.

Figure 3-2 shows a vertical pn junction diode fabricated during the drain/source implants for the p-channel and n-channel MOSFETS. The n^+ substrate contact is connected directly to V_{DD} and reverse biases the pn junction. The photocurrent from carriers generated below the surface of the device is supplied to a load connected at the p^+ region ohmic contact. Other photodetectors have been fabricated and tested as part of this

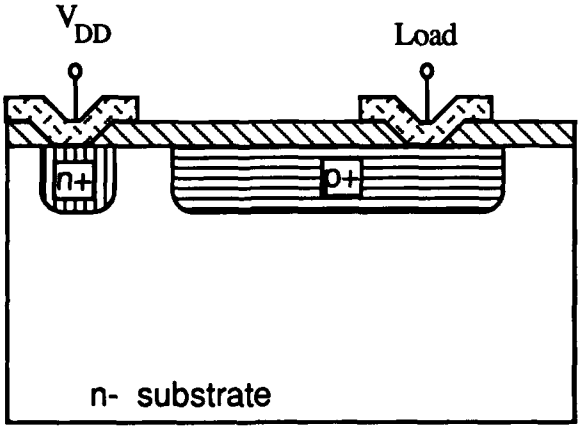


Figure 3-2. Vertical pn Junction Photodiode

research; however, the vertical pn diode is the primary detection device used in the optoelectronic work presented in this thesis. Due the importance of this device, the remainder of this chapter will be devoted to its analysis and model development.

3.2 Analysis of a pn Junction Photodiode

For the pn junction photodiode in Fig. 3-3, the donor concentration in the n- region is much less than the acceptor concentration in the p+ region. Thus, the depletion layer appears mostly in the n- substrate as shown. When photons with energy greater than the bandgap energy (~ 1.1 eV for silicon) are absorbed by the detector, electron-hole pairs are generated in the p+ implant, depletion, and n- substrate regions. Photocurrent flows in the diode when the high electric field across the depletion region causes holes and electrons to drift toward the p+ and n- regions, respectively. The total photocurrent I_P is the sum of the hole and electron currents. Since a large electric field exists only across the depletion layer, carriers generated in the n- bulk region are not immediately included in the drift current. Some of the holes generated in the bulk region, but within a diffusion length of the depletion layer, diffuse to the device junction and contribute to the output photocurrent.

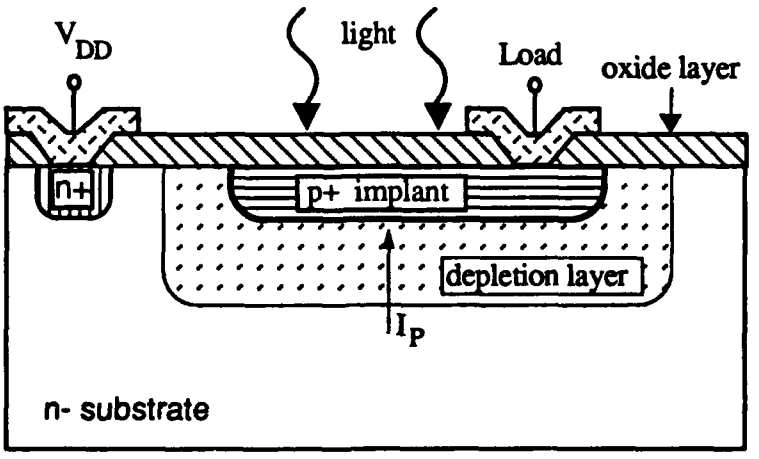


Figure 3-3. Cross-sectional View of a pn Junction Photodiode.

Electrons and holes generated by photon absorption deep in the bulk region may recombine or diffuse away from the junction. In the latter case, crosstalk [55] may affect the operation of other devices in the circuit. Major losses in silicon photodiodes are caused by recombination in the bulk region below the area depleted of free carriers, recombination at the silicon surface, and reflection from the front surface [56].

In the remainder of this section, the static and dynamic characteristics of the pn junction photodiode are addressed. The discussion includes basic diode characteristics, photodetector efficiency, and photodiode model parameters.

3.2.1. Diode Equivalent Circuit

A simple equivalent circuit of a silicon pn junction diode is shown in Fig. 3-4. Resistor R_s includes the series resistance of the p+ implant, the ohmic contacts, and the

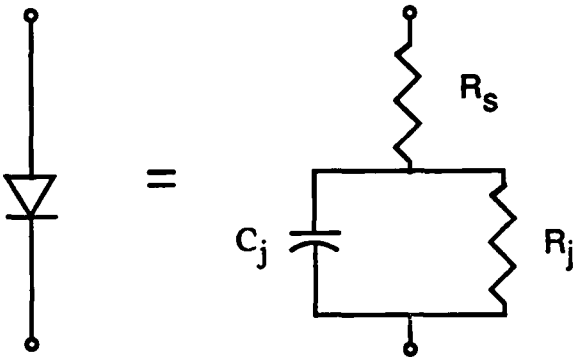


Figure 3-4. Diode Equivalent Circuit [57].

bulk region. The resistance and capacitance of the junction depletion region are shown as R_j and C_j, respectively. For most photodiodes fabricated in a p-well CMOS process, the pn junction is reverse biased when no light is applied. This is due to the requirement that the substrate be connected to the most positive voltage. Under this condition, R_j is much greater than the series resistance and is determined by the bias voltage and reverse current

of the diode. The value of C_j decreases with increasing depletion layer thickness (or increasing reverse bias voltage) and is given by

$$C_j = \frac{\varepsilon_s A}{W} \tag{3.1}$$

where ε_s is the permittivity of silicon, W is the junction depletion layer width, and A is the bottom and sidewall area of the p+ implant. When the pn junction is reverse biased, the depletion layer width is given by

$$W = \sqrt{\frac{2\varepsilon_s}{q}\left(\frac{N_A + N_D}{N_A N_D}\right)(V_{bi} + V_R)} \tag{3.2}$$

where q is the electronic charge, V_{bi} the "built-in" potential across the depletion layer, V_R the externally applied reverse bias voltage, and N_A and N_D the acceptor and donor impurity concentrations, respectively. Using values in Table A-1, W is approximately 3.75 μm when $V_R \approx V_{DD}$=5 volts.

3.2.2 Diode Photocurrent

When a constant light beam is incident on a photodiode, a steady-state current flows in the device. The illuminated photodiode may be modeled simply by adding an independent current source to the circuit in Fig. 3-4 to obtain Fig. 3-5. The theoretical photocurrent I_p in a detector device is generally given by

$$I_p = \eta \frac{qP_o}{h\upsilon} \tag{3.3}$$

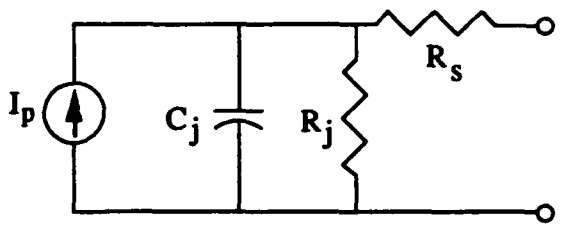


Figure 3-5. Steady-state Model of a Photodiode [26].

where η is the quantum efficiency, P_o is the incident optical power, and $h\upsilon$ is the photon energy [58]. The quantum efficiency, which is defined as the number of electron-hole pairs generated per photon incident on the detector [59], is a function of wavelength [53] and device depth. At light wavelengths near 0.8 μm, the quantum efficiency for silicon can approach 100% when the thickness of the device is at least several light penetration depths. The penetration depth is the point at which the transmission is 0.368 (e^{-1}). In a CMOS integrated circuit, this requirement is not met since the typical junction depth is only about 0.5 μm, while the light penetration depth for silicon is approximately 10 μm [22]. Published quantum efficiency data [53] only applies directly to devices greater than 6.5 penetration depths in thickness. For example, when the device depth is 6.6 penetration depths the possible absorption rate is 99.9%. Although a detector in a CMOS circuit may potentially have a high absorption rate, the photons absorbed deep in the substrate are included in quantum efficiency, but are not converted to output current. Thus, both internal and external quantum efficiency [54, 60] are required for determination of the photocurrent in detectors addressed in this chapter.

A more precise expression for the photocurrent in a shallow detector is [26]

$$I_p = \left[\frac{qP_o}{h\upsilon}\left(\frac{A_d}{A_b}\right)(1-r)\right](1-e^{-\alpha x}) \qquad (3.4)$$

where A_d and A_b are the detector area and incident light beam area, respectively. These two parameters are used when the detector area is less than the incident beam area; the ratio cannot be greater than unity. The reflection coefficient (r) applies to reflection at the detector surface, while α and x are the absorption coefficient and penetration depth into the device, respectively. For shallow photodetectors, the penetration depth in equation (3.4) refers to the largest penetration at which photon-generated carriers contribute to the current, instead of the total depth of photon absorption. The photocurrent is discussed in more detail in a later section.

3.2.3 Photodiode Transient Response

As described above, a portion of the holes generated in the substrate are expected to diffuse to the edge of the depletion layer. A shortcoming of equation (3.4) is that it provides no information on the time for hole diffusion. The hole diffusion time t_p is expressed as [39]

$$t_p = \frac{L_p^2}{D_p} \tag{3.5}$$

where L_p is the hole diffusion length and D_p is the hole diffusion constant. A typical value for D_p in lightly doped silicon is 13 cm^2/s [61]. The hole diffusion length is significantly greater than the depletion layer width of vertical photodiodes investigated in this chapter. The time required for holes to diffuse to the edge of the depletion layer limits the transient response of high speed optoelectronic systems.

The speed of an optoelectronic circuit is also limited by the time constant of the detector circuit and load. Figure 3-6 shows a load capacitor C_L and resistor R_L added to the photodetector model of Fig. 3-5. Neglecting the series resistance R_s, the time constant τ

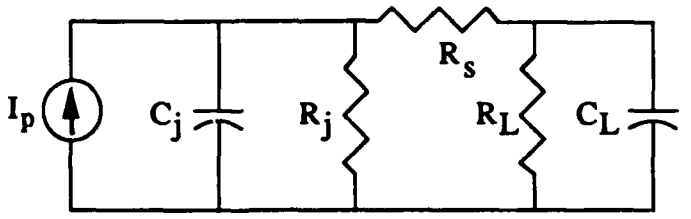


Figure 3-6. Model for Detector Circuit with RC Load.

may be written as

$$\tau = (R_j \| R_L)(C_j + C_L) \tag{3.6}$$

where R_j and C_j are both functions of the reverse bias voltage applied to the detector. The voltage dependence of these parameters effects the transient response in a manner that is not included in the model.

3.3 Development of Improved Photodetector Models

Husain [16] and Goodman et al. [9] suggested optical systems as a means of overcoming interconnect problems in VLSI circuits. Prior to that time, the diode small signal model adequately emulated pn junction photodetectors in most applications [58, 62]. The emergence of optical interconnects and related technologies such as optical ROM-to-electronic RAM data transfer has introduced a need for models which better approximate large signal operation of a photodetector. Other than piecewise-linear models [63], few special techniques are available for large signal modeling of reverse biased diodes. However, development of an ideal photodetector model is not the intent of this chapter. A practical model need only provide accurate theoretical and simulation results within constraints defined by the user. The required accuracy depends on the application for the device.

A simple photodiode model was described in Section 3.2. The in-depth discussion of the photodetection process in this section will be the basis of several proposed improvements to photodiode models. This treatment of photodetection devices focuses on the flow of current in a pn junction diode during dark conditions as well as illumination.

3.3.1 Average Diode Capacitance

The photodiode junction capacitance is a function of the reverse bias voltage applied to the detector. As the depletion layer width decreases, C_j increases. The potential increase in junction capacitance may be significant to the response of the detector circuit. Using typical parameters for a 2 μm CMOS process , the junction capacitance of a 10 μm x 10 μm detector with a junction depth of 0.5 μm is calculated to be approximately 3.4 fF when the photodetector reverse bias is 5 volts. As V_R decreases towards zero, C_j approaches 9 fF, which is an increase of 166%. The capacitance of the 10 μm x 10 μm detector is shown as a function of reverse bias voltage in Fig. 3-7. In small signal models, the DC operating point determines the capacitance value, which may be taken as constant for small voltage variations. This approximation does not hold for large signal applications. Thus, the depletion capacitance must be approximated by a polynomial, by piecewise-linear values, or perhaps by the linear average value described below.

The average value of capacitance may be defined as the total change in charge on the capacitor as voltage varies from one value to another, divided by the voltage change [64]. The average capacitance value when V_R changes from V_1 to V_2 may be written as

$$C_{AV} = \frac{Q(V_2) - Q(V_1)}{V_2 - V_1} \tag{3.7}$$

where $Q(V_1)$ and $Q(V_2)$ are the values of charge on the capacitor at the respective voltages.

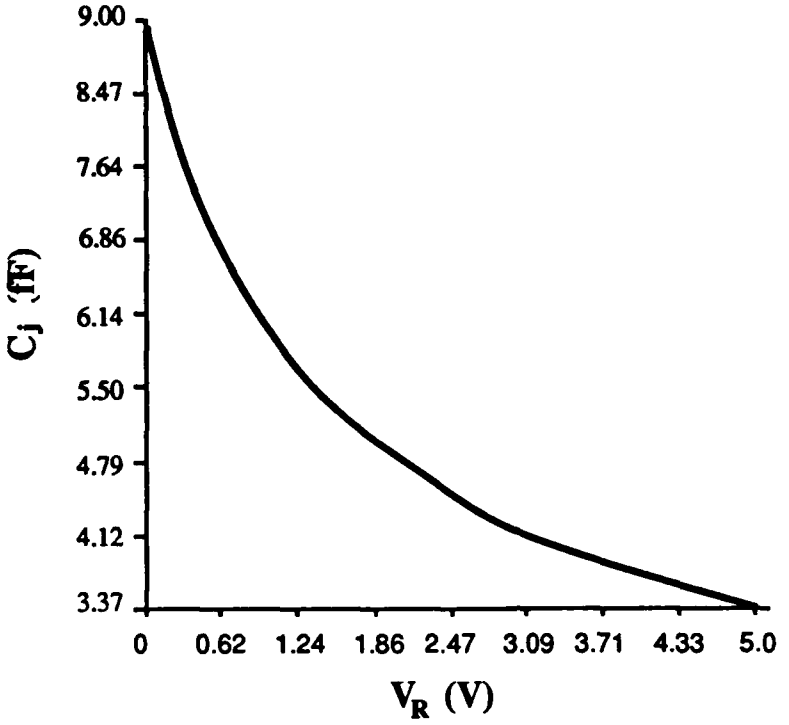


Figure 3-7. Junction capacitance as a function of reverse bias voltage for a 10 μm x 10 μm photodetector.

The total change in charge is

$$Q = \int_{Q_1}^{Q_2} dQ = \int_{V_1}^{V_2} \frac{dQ}{dV} dV = \int_{V_1}^{V_2} C_j \, dV \tag{3.8}$$

where C_j is the junction capacitance of the diode as defined in equation (3.1) and V is used in place of V_R for convenience. The average capacitance can now be written as

$$C_{AV} = \frac{\int_{V_1}^{V_2} C_j dV}{V_2 - V_1}. \tag{3.9}$$

Substituting equations (3.1) and (3.2) and performing the integration, gives the average value of capacitance for an abrupt pn junction as

$$C_{AV} = \frac{A\sqrt{2\varepsilon_s q N_D}}{(V_2 - V_1)}\left[(V_{bi} + V_2)^{\frac{1}{2}} - (V_{bi} + V_1)^{\frac{1}{2}}\right] \tag{3.10}$$

where $N_A >> N_D$ and $V_2 > V_1$ have been assumed. Typically, V_1 is the dark output voltage of the detector and V_2 the maximum output during illumination. This expression for capacitance can be used as a parameter for an improved photodiode model.

3.3.2 Photocurrent Approximation

The relationships between photon absorption, device junction depth, and current were briefly discussed in Section 3.2.2. In this section, photon absorption in a pn junction diode and the components of equation (3.4) will be further investigated.

Figure 3-8 is a plot of absorption coefficient and penetration depth as a function of wavelength for silicon. It is evident that for most of the wavelengths shown, the light penetration depth is greater than the junction depth of a photodiode in a CMOS circuit. Thus, the exponential term in equation (3.4) is necessary to determine the fraction of incident photons that are absorbed in the vicinity of the junction of a shallow photodiode.

The photocurrent for a shallow detector may be calculated using equation (3.4) and Fig. 3-8 when the wavelength of the incident light or the absorption coefficient is known. Since the light penetration goes well beyond the depth of the junction depletion layer, assumptions must be made concerning the contribution of diffused carriers to the total current. The most common approach is to let the active region of the detector be the depletion layer plus the part of the substrate that is within one diffusion length of the edge

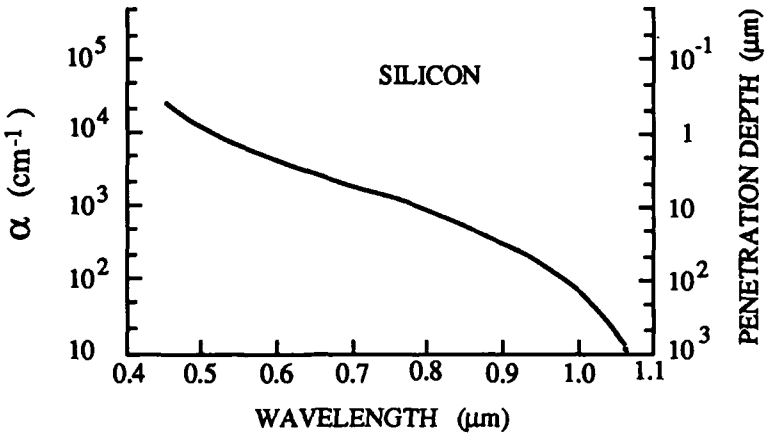


Figure 3-8. Absorption Coefficient and Penetration Depth for Silicon [56].

of the depleted area, i.e., $x = W + L_p$ [55]. This neglects the bottom portion of the substrate, the detector surface, and the p^+ implant. Since the diffusion length is the average distance a carrier is expected to travel in one direction, the actual length the active region extends into the substrate depends on the geometry of the device. Absorption at the surface and p^+ regions may be accounted for by multiplying equation (3.4) by $\exp(-\alpha x_j)$, where x_j is the junction depth. It can be shown that only about 5% of the photons are absorbed above the junction. Some of the holes generated in those regions recombine with electrons at the surface.

The transmittance (1-r) is the percentage of incident photons penetrating the silicon surface, where the reflectance (r) is the percentage of light reflected. Generally, when light is at normal incidence, the reflectance at the boundary between two media of refractive indices n_0 and n_1 is determined by [65]

$$r = \left(\frac{n_1 - n_0}{n_1 + n_0} \right)^2 . \tag{3.11}$$

The reflectance between air ($n_0 = 1$) and silicon ($n_1 = n_{Si} \approx 3.5$) [61] is approximately 30%. However, when an antireflection coating having an index of

$$n = \sqrt{n_0 n_1} = \sqrt{n_{Si}} \approx 1.9 \tag{3.12}$$

and a thickness of a quarter wavelength is applied to the silicon surface, the reflectance is reduced to near zero. The oxide layer on the surface of a silicon wafer serves as a good antireflection coating since it has a refractive index between 1.45 and 1.9 [53, 66]. Thus, neglecting the reflectance r in equation (3.4) may be acceptable based on the value of the oxide layer refractive index.

Equation (3.4) neglects the changes in depletion layer width during the detection process. The depletion region decreases during the detection process due to the increase in the number of free carriers in the substrate. The depletion layer also decreases when the reverse bias voltage across the diode decreases. This occurs during the detection process as the detector load voltage increases. The expression for photocurrent given in equation (3.4) for a shallow detector becomes a function of depletion width as well as reverse bias voltage when the light penetration depth is replaced by $(W + L_P)$. Equation (3.4) is then written as

$$I_p = \left[\frac{qP_o}{h\upsilon}\left(\frac{A_d}{A_b}\right)(1-r)\right]\left(1 - e^{-\alpha(W+L_P)}\right) \tag{3.13}$$

and solved at a specific value of voltage by replacing W by the depletion width given in equation (3.2). Since the voltage across the detector changes as the load capacitor charges, simulation of the photodiode operation requires calculation of the depletion layer width at

each time point. Using SPICE to simulate a photodetector circuit requires either a concurrent iterative analysis or a set of approximations for equation (3.13) which may be used directly in the input file.

3.3.2.1 Exponential Series Approximation

A simple approximation [55] is obtained by using an exponential series expansion and neglecting higher order terms. Equation (3.13) is then written as

$$I_p = \left[\frac{qP_o}{h\upsilon}\left(\frac{A_d}{A_b}\right)(1-r)\right]\left(1-\frac{e^{-\alpha L_p}}{1+\alpha W}\right). \tag{3.14}$$

Treating $\exp(-\alpha L_P)$ as a constant, leaves equation (3.14) without an exponential term; however, the function is still not linear since the depletion width is a function of the square root of the reverse bias voltage. The series expansion approximation is valid when the dopant concentration in the substrate is such that $\alpha W << 1$. As shown in Fig. 3-9, equation (3.14) deviates from equation (3.13) when the depletion layer width is large. The graph is based on parameters in Table A-1, which shows a relatively low value for the substrate concentration. The maximum depletion layer width calculated from values in the table is approximately 4 μm. Because of the strong dependence on the fabrication process, equation (3.14) is not necessarily a good approximation for I_P.

3.3.2.2 Polynomial Approximation

For SPICE simulations, the photocurrent may be characterized as a nonlinear dependent current source with the diode reverse bias voltage as an argument. This is possible if the exponential term in equation (3.13) is replaced by a polynomial approximation. The resulting one-dimensional voltage-controlled current source may be entered directly into a SPICE input file. By combining the terms in equation (3.13) which

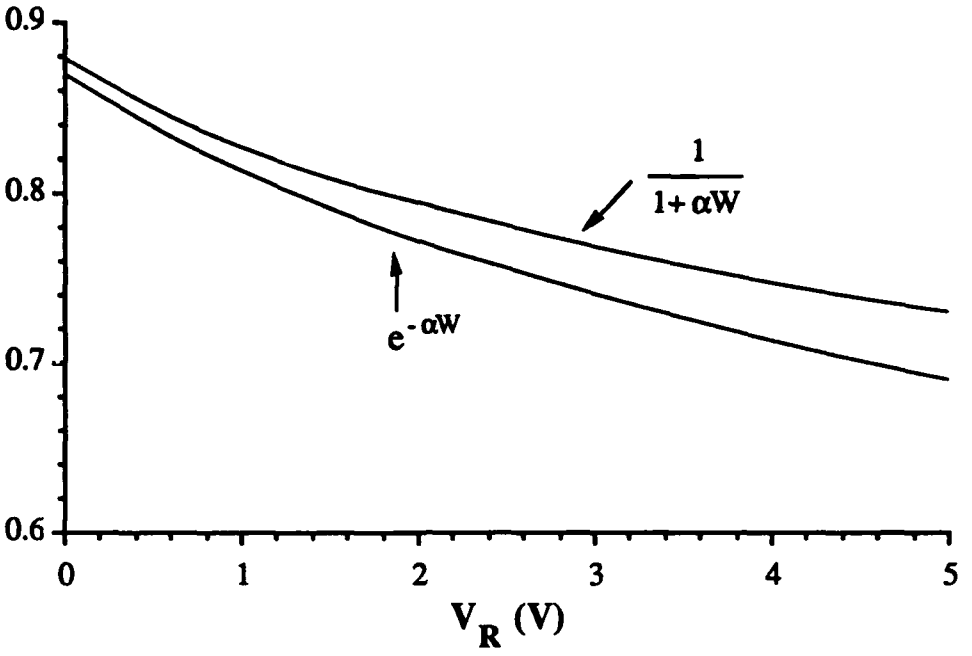


Figure 3-9. Plot of Exponential and the Series Approximation.

have no voltage dependence, the photocurrent can be written as

$$I_p = K\left(1 - e^{-\alpha (W + L_P)}\right) \tag{3.15}$$

where

$$K = \left[\frac{qP_o}{h\upsilon}\left(\frac{A_d}{A_b}\right)(1 - r)\right]. \tag{3.16}$$

Equation (3.15) is plotted in Fig. 3-10 with K normalized to unity for convenience. The change in normalized photocurrent shown in the figure can be approximated by a second order polynomial with a small error, or a third order polynomial with negligible error.

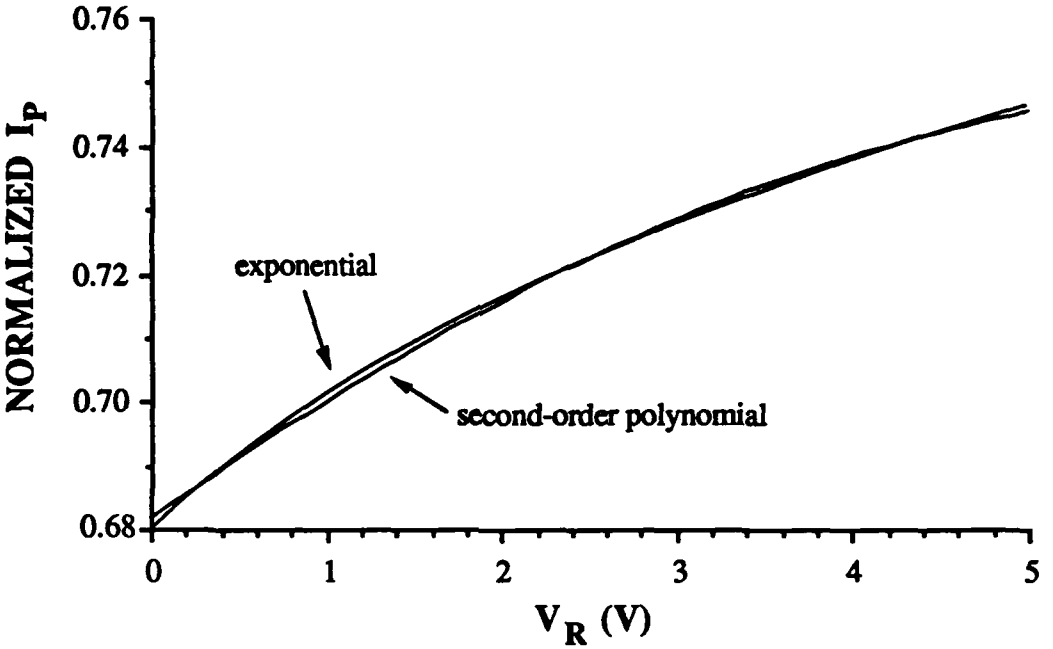


Figure 3-10. Normalized Photocurrent. The exponential curve and the second order polynomial approximation are shown. The third order polynomial approximation coincides with the exponential curve. L_p=10 μm and α=1.0 μm.

For the third order polynomial approximation, the curve fitting procedure gives

$$\left(1 - e^{-\alpha(W+L_P)}\right) \approx 2.63V_R^3 - 3.41V_R^2 + 2.37V_R + 0.68 \ . \tag{3.17}$$

The photocurrent is then written as

$$I_P \approx 2.63(K)V_R^3 - 3.41(K)V_R^2 + 2.37(K)V_R + 0.68(K) \ . \tag{3.18}$$

This expression is then entered into a SPICE input file with the reverse voltage across the diode as the control parameter.

3.3.2.3 Constant Value Approximation

A constant value approximation of the photocurrent may be obtained by finding the linear average depletion width using a method similar to that used for the junction capacitance in Section 3.3.1. The resulting average depletion width [51] is given as

$$W_{AV} = \frac{2}{3(V_2 - V_1)}\sqrt{\frac{2\varepsilon_s}{qN_D}}\left[(V_{bi} + V_2)^{\frac{3}{2}} - (V_{bi} + V_1)^{\frac{3}{2}}\right] \tag{3.19}$$

where V_1 and V_2 are the lower and upper limits for the reverse bias voltage across the diode. Both values are positive according to the convention described previously. Substitution of equation (3.19) into equation (3.13) gives an average value of photocurrent which may be used as a constant independent current source in a SPICE simulation.

3.3.3 Dark Current

In the absence of light, the current in a diode is the combined hole and electron current of the pn junction and is given by the Shockley diode equation [67]

$$I_D = I_0\left(e^{V/V_T} - 1\right) \tag{3.20}$$

where V is the externally applied voltage, V_T is the thermal voltage, and I_0 is the reverse saturation current. When the diode is reverse biased (V<0), the exponential term in equation (3.20) becomes small and usually may be neglected. This gives the magnitude of the reverse current as approximately equal to the reverse saturation current. Since I_O flows in the reverse direction in the diode, it adds to the photocurrent determined by equation (3.4). Typically, I_O is several orders of magnitude smaller than the photocurrent in practical devices and is often neglected in detector models. However, the reverse saturation

current is included in noise equivalent circuits [53] since it affects the minimum detectable signal.

According to the Shockley diode equation, the dark current should be approximately equal to the reverse saturation current. To more realistically model the behavior of a reverse biased silicon diode, the current due to generation and recombination in the depletion region must also be included in the dark current [53, 68]. In a silicon diode at room temperature, generation dominates recombination and causes a current which is much greater than the reverse saturation current [51]. Thus, I_O can generally be neglected for the photodetector applications in this thesis since the dark current is approximately equal to the generation current.

The static photodiode model in Fig. 3-5 can be improved by including the generation current. This is particularly true when the detector load resistor is large or when the photocurrent is on the order of the dark current. The generation current can be modeled as a nonlinear source or as an average-valued constant source. The nonlinear function can be found by applying a curve-fitting procedure to the changing depletion layer width. However, an average value approximation is practical since the photocurrent usually dominates when the depletion layer width changes during the detection process.

The generation current I_{GEN} is given by

$$I_{GEN} = \frac{qn_i WA}{\tau_e} \tag{3.21}$$

where n_i is the intrinsic carrier concentration, W is the depletion width, and τ_e is the effective carrier lifetime [68]. The effective lifetime may be approximated by the sum of the hole and electron lifetimes ($\tau_p + \tau_n$) [51]. The average generation current can be

determined by replacing W in equation (3.21) by the linear average depletion width of equation (3.19).

Besides being a function of depletion width, the dark current is also a strong function of temperature [59]. For example, when the energy of the incident light significantly exceeds the bandgap energy, an excessive number of thermally generated carriers result in a larger dark current [55] when the light is removed. The thermally generated current is more difficult to model due to its dependence on the optical source. Although it is acknowledged here, thermal current is not included in the models presented in this chapter.

3.3.4 Average Junction Resistance

The diode junction resistance is equal to the reverse bias voltage divided by the current flowing in the device. Under dark conditions the resistance is defined by

$$R_j = \frac{V_R}{I_{GEN}} \tag{3.22}$$

where I_{GEN} is calculated from equation (3.21) and the diode reverse saturation current is neglected. When $V_R=V_{DD}$ and I_{GEN} is calculated from the average depletion layer width, the average junction resistance becomes

$$R_{AV} \approx \frac{V_{DD}}{I_{GEN}} \ . \tag{3.23}$$

The junction resistance can also be approximated by a nonlinear dependent current source. A polynomial approximation of I_{GEN} with V_R as an argument becomes a nonlinear resistor when the source nodes are the same as the controlling nodes. The junction resistance

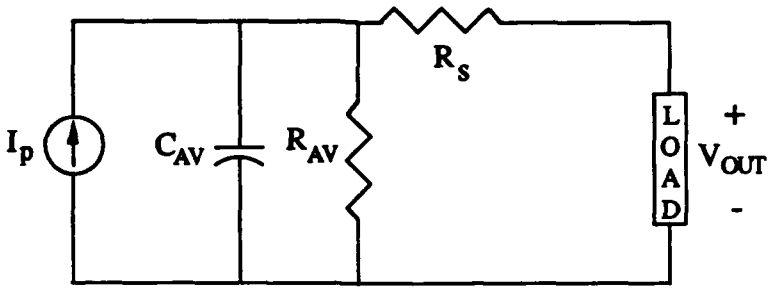
would be replaced by a current source, with the voltage across the current source as the control parameter.

3.3.5 Proposed Photodiode Models

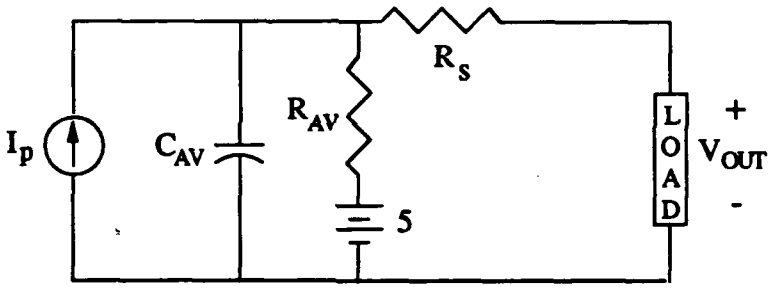
Based on the discussion in this chapter, two models are proposed for SPICE simulation of pn junction photodiodes fabricated in a CMOS process. The original equivalent circuit model discussed in Section 3.2, and the two new models are shown in Fig. 3-11. Average values have been substituted for the original junction parameters. These models may be further improved by use of the polynomial approximations for the photocurrent and junction resistance described previously. Parameters for the discrete element and diode models are summarized in Table 3-1.

The SPICE circuit simulator was used to determine the transient response of each of the three models in Fig. 3-11. The simulated device is a photodiode fabricated in a 2 μm p-well CMOS process. The results are for a 10 μm x 10 μm detector when the incident light power is 20 μW at a wavelength of 0.63 μm. Figure 3-12 shows the transient response of the respective models when the load resistance is 1 MΩ and the capacitance is 20 fF. All of the results are similar since the load resistance is too small for the dark current of the photodetector to cause a measurable DC output voltage. The dark output voltage must be included in the simulations since the detectors are used to drive devices having an input threshold voltage.

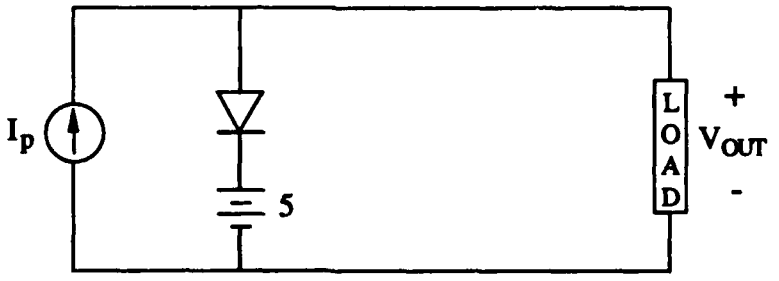
For the simulation results shown in Fig. 3-13, the load resistance was increased to highlight the difference between the models when the dark current is included. The equivalent circuit model has a zero DC output voltage since it does not account for the diode reverse current. The discrete element and diode models show a small DC output voltage because the dark current is included in the model. Approximately the same DC output voltage was obtained for both models by calculating the junction resistance of the discrete



(a) Equivalent Circuit Model



(b) Discrete Element Model



(c) Diode Model

Figure 3-11. Photodiode Models for SPICE Simulations.

Table 3-1. Photodiode Model Parameters

(a)

DISCRETE ELEMENT MODEL PARAMETERS
$W_{AV} = \frac{2}{3(V_2 - V_1)}\sqrt{\frac{2\varepsilon_s}{qN_D}}\left[(V_{bi} + V_2)^{\frac{3}{2}} - (V_{bi} + V_1)^{\frac{3}{2}}\right]$
$I_p = \left[\frac{qP_o}{h\omega}\left(\frac{A_d}{A_b}\right)(1-r)\right]\left(1 - e^{-\alpha (W_{AV}+L_P)}\right)$ or polynomial
$C_{AV} = \frac{A\sqrt{2\varepsilon_s qN_D}}{(V_2 - V_1)}\left[(V_{bi} + V_2)^{\frac{1}{2}} - (V_{bi} + V_1)^{\frac{1}{2}}\right]$
$I_{GEN} = \frac{qn_i W_{AV} A}{\tau_e}$
$R_{AV} = \frac{V_{DD}}{I_{GEN}}$ $\quad R_s = 10\Omega - 1K\Omega$

(b)

DIODE MODEL PARAMETERS	
$IS = qA n_i^2\left(\frac{D_P}{L_P N_D}\right)$	$R_s = 10\Omega - 1K\Omega$
$CJO = A\sqrt{\frac{\varepsilon_s q N_D}{2 V_{bi}}}$	VJ = 0.86 M = 0.5

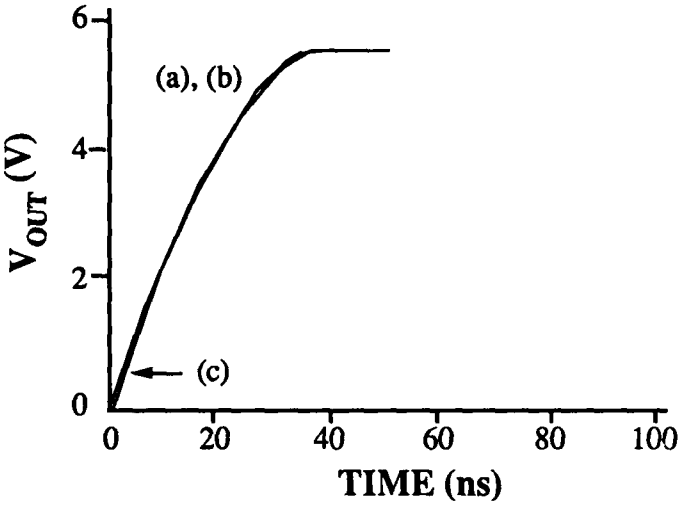


Figure 3-12. Transient Response of Photodiode Models. (a) Equivalent circuit model. (b) Discrete element model. (c) Diode model.

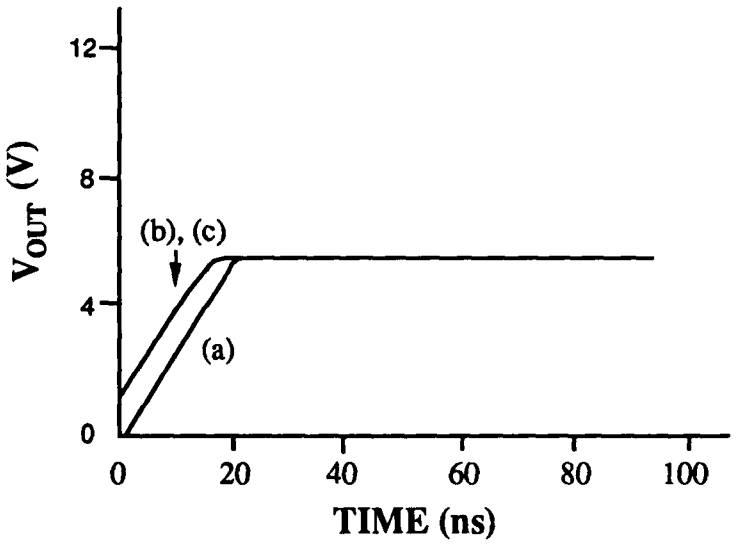


Figure 3-13. Transient Response of Photodiode Models. The effects of the dark current are shown. (a) Equivalent circuit model. (b) Discrete element model. (c) Diode model.

element model from the generation current instead of the reverse saturation current. The discrete element and the diode models also gave similar results in the transient analysis.

The discrete element model and the diode model are recommended based on the results discussed in this section. The two models are designed to approximate the voltage dependence of model parameters. Although the diode model is easier to implement, the discrete element model offers more insight into the physical operation of the detector as well as its limitations.

3.4 Experimental Results

The DC characteristics of two photodetectors were determined using the experimental setup described in Appendix B. Although the experimental portion of this research is primarily intended to support concepts presented in later chapters, some of the results are reported here to provide representative values for the dark current and photocurrent flowing in a detector. The layouts for a vertical pn junction photodiode and a vertical npn transistor are shown in Fig. 3-14. Substrate contacts are used to form a guard ring on three sides of the light sensitive regions. Both the p^+ implant of the diode and the p-well diffusion of the transistor measure 50 μm x 50 μm. The n+ implant of the vertical transistor is 32 μm x 26 μm. For both devices, the substrate and guard ring are connected to a 5 volt power supply. The transistor is connected as a diode since the n^+ implant is also tied to V_{DD}. The dark current was measured at 34.4 pA and 36.94 pA for the diode and the transistor, respectively. With the room lights on, the respective measurements were 1.04 nA and 1.3 nA. The dark current for both devices is within the range of values expected for the generation current. The circuit shown in Fig. 3-15 was used to measure the responsivity of the pn junction photodiode. The voltage drop across a 200 kΩ resistor was measured with a voltmeter, while the laser power was monitored. The photocurrent and responsivity are shown in Fig. 3-16. The measured responsivity is 0.178 A/W.

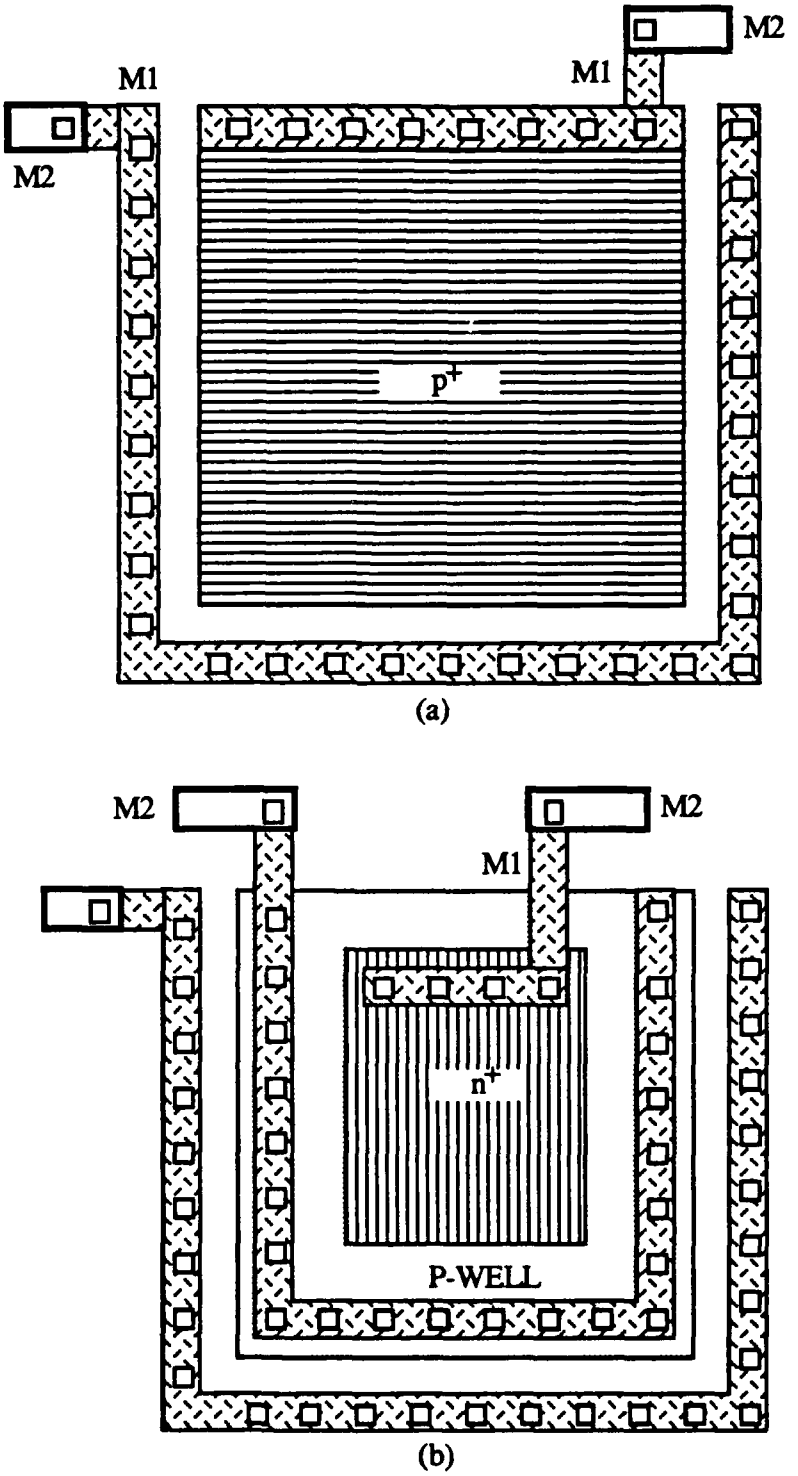


Figure 3-14. Photodetector Layouts. (a) Vertical diode. (b) Vertical npn transistor.

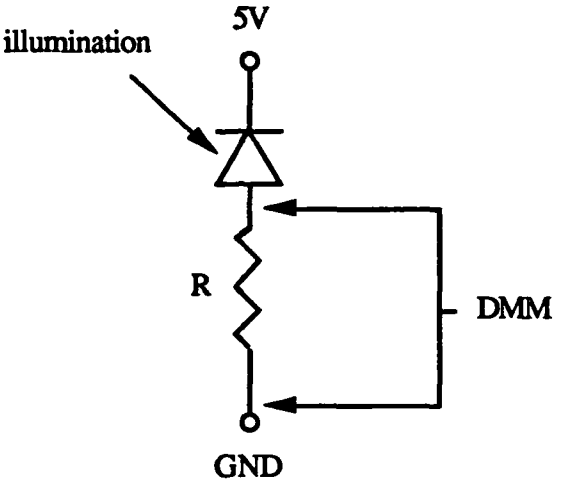


Figure 3-15. Circuit Schematic for Measuring the Response of a Photodiode.

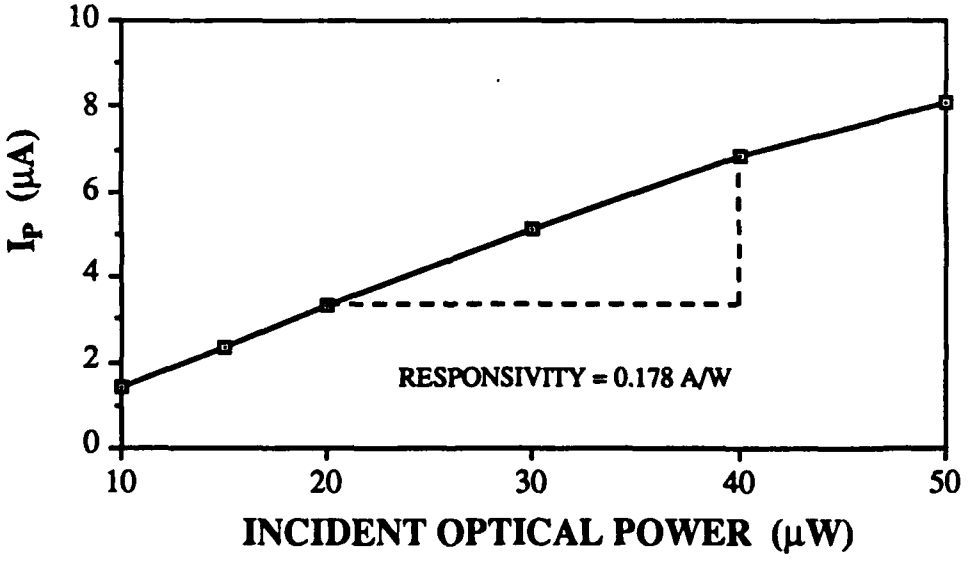


Figure 3-16. Photocurrent Response of a Vertical pn Junction Photodiode.

3.5 Chapter Summary

Several photodetection devices which are compatible with bulk CMOS fabrication processes have been presented in this chapter. General requirements for modeling such devices have been discussed and related to specific models for SPICE simulations. A vertical pn junction photodiode was analyzed and used as a basis for reporting simulation and experimental results. In the next chapter, these photodetectors will be coupled with CMOS devices to form a variety of optoelectronic circuits.

CHAPTER 4

OPTICAL DATA DETECTION CIRCUITS

The two previous chapters discussed the design and analysis of CMOS static RAM cells and the geometry of photodetectors that can be fabricated in a bulk CMOS process without additional process steps. In this chapter the photodetectors are combined with load devices which convert the optical information received by the detector into a DC output voltage. Some of these circuits are used as optical inputs for the optoelectronic storage circuits presented in Chapter 5.

A photodiode with an unspecified load device is shown in Fig. 4-1. For the applications presented in this thesis, a load with a high resistance and a low capacitance is preferred. A high resistance load device is necessary to keep the photocurrent and the total laser power at practical levels. The detectors discussed in this chapter will be configured in an array to allow transfer of optical data from a holographic ROM containing a large number of bits. Since the ROM is driven by a single light source, a small increase in the

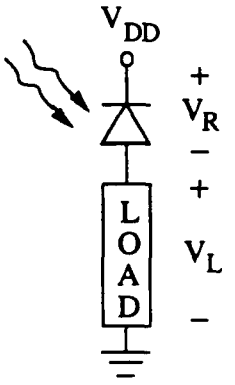


Figure 4-1. Photodiode with a Load Device.

required optical power per bit may result in a large increase in total laser power. Thus, one of the objectives in designing a detector load or pull-down device is to obtain the largest possible load voltage V_L from a small diode current.

Besides a large resistance, a small capacitance is also desired. The transient response is a primary concern for detector circuits used in optical ROM-to-electronic RAM data transfer applications. A simple transient analysis of a detector with a capacitive load can be derived from $i = C\,(dv/dt)$ calculations. For a fixed charging current and detector capacitance, the response time can be improved by minimizing the capacitance of the detector load. The capacitance is determined by the choice of load device as well as the fabrication process and the geometry of the layout. Although using a larger photocurrent will also reduce the response time, this is not an acceptable alternative since the current per pixel must be kept small when the detector array is large.

A third consideration in selecting a photodetector load device is the discharge time of all capacitive elements connected to the output node of the detector pull-down device. This corresponds to the fall time of the transient response curve after the light source is shut off. In Fig. 4-2, the dark current of the detector is approximated by the generation current I_{GEN}.

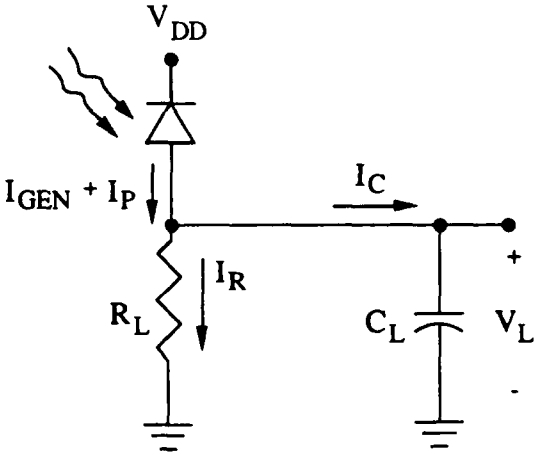


Figure 4-2. Photodetector and RC Load.

When the light source is active, the photocurrent is much greater than the dark current and $I_P \approx I_R + I_C$. After the light is turned off, I_C becomes negative since C_L must discharge. Since the photocurrent is zero, then $I_{GEN} + I_R = -I_C$ or $I_R \approx -I_C$. If R_L is a large fixed resistor, C_L will discharge slowly. If R_L is reduced, the RC time constant will be smaller, but the photocurrent required during the charge cycle may be too large. Neither of these two conditions is desirable. For a practical optoelectronic circuit, the preferred load device is a nonlinear resistor. For small values of output voltage, the resistance needs to be large, such that a small photocurrent causes V_L to rise to a designated threshold (e.g. 1V). When the output voltage is increased, the resistance must be small enough to allow C_L to quickly discharge below the same threshold voltage.

In the remainder of this chapter, a variety of photodetector load devices are analyzed. Simulation and experimental results are provided for some circuits. All MOSFETs used as load devices are enhancement type transistors. Silicon devices used for experimentation were fabricated in a 2 μm p-well CMOS process.

4.1 Saturated PMOS Transistor Load

A photodiode with a saturated p-channel transistor load is shown in Fig. 4-3 [28, 51]. This detector and pull-down load configuration has provided the best results for optical data transfer applications. Conduction in a PMOS device is based on a channel formed by holes, which have a lower mobility μ_p than electrons. This is an advantage over an NMOS device since the increased channel resistance provides a larger voltage change for a given value of photocurrent. However, since the mobility of holes is lower, using a PMOS load transistor slows the transient response of the detector circuit [51]. The smaller value of μ_p most critically affects the fall time of the response curve after the light source is turned off.

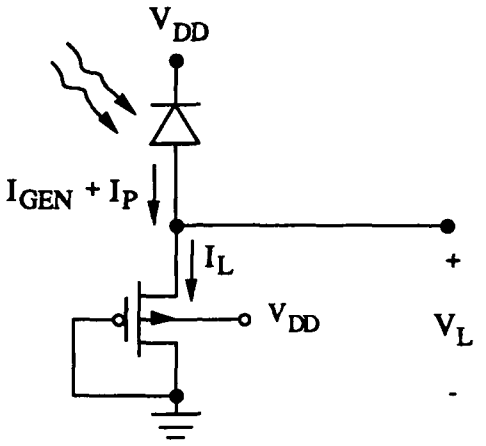


Figure 4-3. Photodiode with a Saturated PMOS Transistor Load.

Using the SPICE circuit simulator and the model parameters given in Table A-1, a transient response was obtained for the detector and PMOS load transistor in Fig. 4-3. The results are shown in Fig. 4-4 for $(W/L)_P = 3/20$ and p^+n^- detector dimensions of 30 μm x 30 μm. The response is for an input photocurrent pulse which has a rise and fall time of 1 ns and a pulsed value of 10 μA as shown in Fig. 4-5.

The PMOS load is biased in the active mode of operation since the gate is connected to ground. With the device biased such that $|V_{GS}| > |V_{Tp}|$, an inversion layer of holes forms a conducting channel from the source to the drain of the transistor [51]. The lowest value of V_L occurs under dark conditions, when the output is approximately equal to the PMOS device threshold voltage [28]. The p-channel MOSFET threshold voltage V_{Tp} is determined by [51]

$$V_{Tp} = V_{TOp} - \gamma_p \left(\sqrt{V_{BSp} + 2|\phi_F|} - \sqrt{2|\phi_F|} \right) \tag{4.1}$$

where V_{TOp} is the device threshold voltage without body bias effects, γ_p is the bulk threshold parameter, V_{BSp} is the bulk-source voltage, and ϕ_F is the bulk Fermi potential.

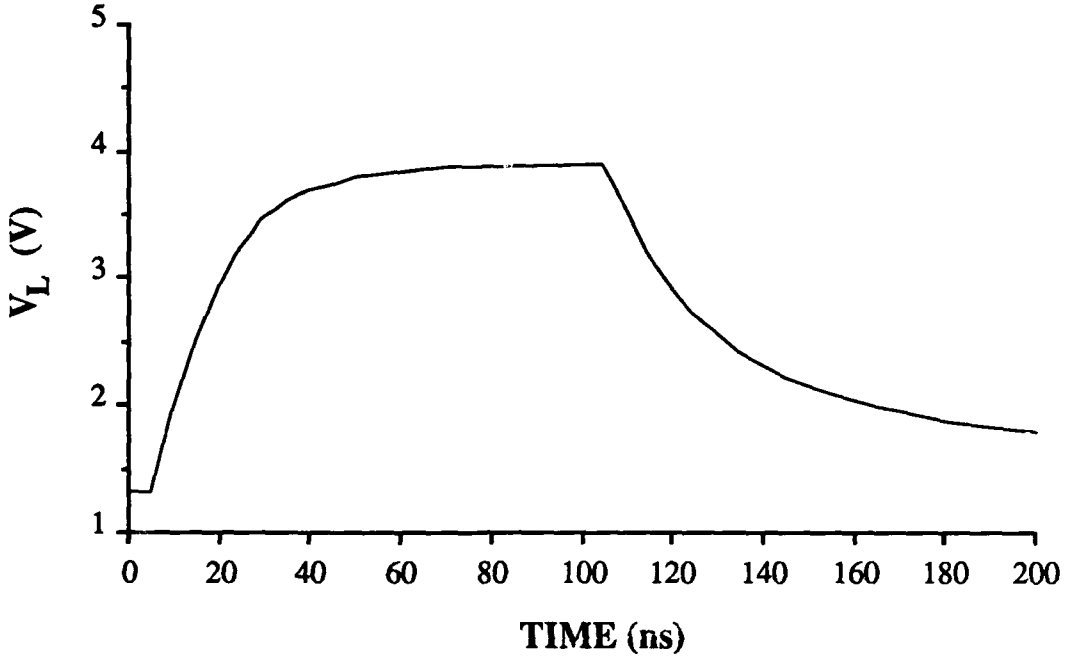


Figure 4-4. Transient Response of the Detector and PMOS Load.

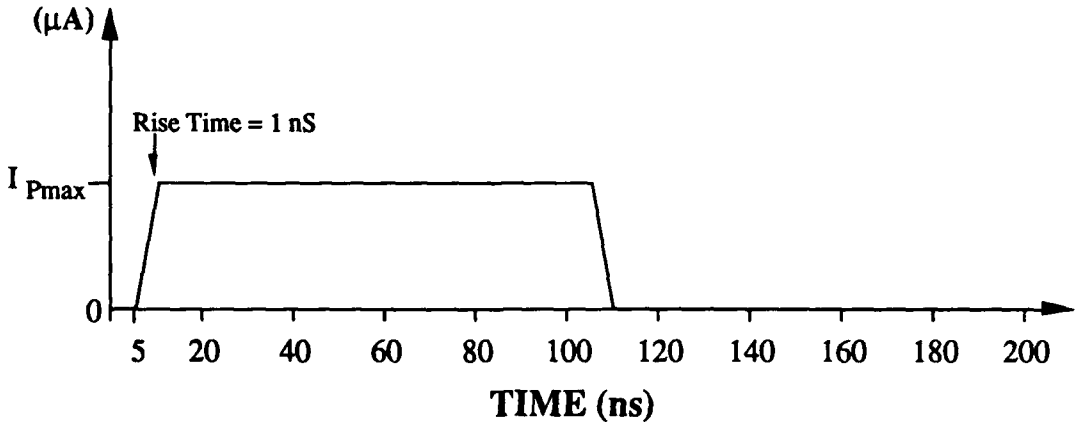


Figure 4-5. Input Photocurrent for Photodiode Circuit Simulations

threshold parameter, V_{BSp} is the bulk-source voltage, and ϕ_F is the bulk Fermi potential. Since V_{BSp} is non-zero, the effects of the bulk bias voltage must be included in the threshold voltage. The bulk is normally connected to the positive supply rail.

An approximate dark output voltage can be calculated by assuming the source voltage V_S is equal to V_{Tp}. Setting $V_{BS} = V_B - V_S$, this gives

$$V_S = V_{TOp} - \gamma_p \left(\sqrt{V_{DD} - V_S + 2|\phi_F|} - \sqrt{2|\phi_F|} \right) \tag{4.2}$$

where $V_B = V_{DD}$ has been used. When the appropriate parameters from Table A-1 are substituted, the iterative solution gives $V_S = V_L = 1.22$ volts. This value is the minimum input voltage to any circuit driven by the detector circuit. Although device threshold voltages may be controlled by the fabrication process, the low value for V_L is too large to keep some state-of-the-art CMOS devices in cutoff. However, it will be shown in the next chapter that this condition has advantages as well as disadvantages when applied to static optoelectronic storage circuits.

SPICE simulation results for the photodetector circuit give a static output voltage of 1.33 volts, while experiments give $V_L \approx 1.43$ V in the presence of room lights, and 1.3 volts in the dark. The experimental results are for a 16 μm x 16 μm p^+n^- detector and a p-channel transistor load with an aspect ratio of $(W/L)_p = 3/31$. When referring to experimental results in this chapter, the expression *under dark conditions* simply implies the absence of laser light. Unless stated otherwise, the fluorescent room lights are left on during the experiment.

Inspection of Fig. 4-4 shows that V_L quickly rises from 1.33 volts to approximately 3.5 volts. Detector circuit output voltages above this level are not a primary concern because normal optical data transfer will have taken place at some lower output voltage.

detector circuits discussed in this chapter are for parallel write operations, rise and fall times under 100 ns are acceptable. This is explained in more detail in Chapter 5.

4.2 Nonsaturated NMOS Transistor Load

Although the nonsaturated NMOS transistor load is similar to the PMOS load, several fundamental differences exist. To bias the n-channel device in the active mode, the gate is connected to the supply rail as shown in Fig. 4-6. The drain-source voltage of the NMOS device is approximately zero under dark conditions. However, since the gate is connected to V_{DD} and the source is grounded, an inversion layer conduction path exists in the channel at all times. When $V_L < (V_{DD} - V_{Tn})$, the photocurrent flows through the resistance of an n-channel transistor in the linear region of operation. In general, the channel resistance of an NMOS transistor is less than the resistance of a PMOS device since the electron mobility μ_n is greater than μ_p. As a result of the difference in mobility and the low static output voltage, the photocurrent required for the NMOS load device is greater than the current required for the PMOS transistor.

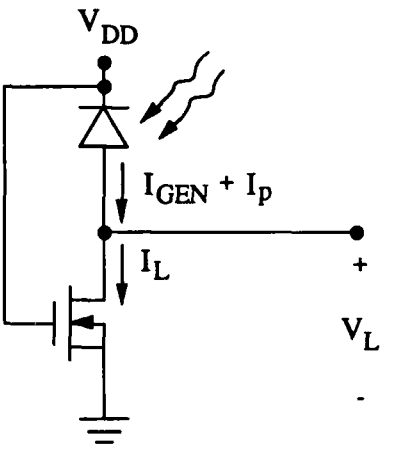


Figure 4-6. Photodiode with a Nonsaturated NMOS Transistor Load.

Figure 4-7 gives the transient response of the circuit in Fig. 4-6. The transistor aspect ratio is the same as in the previous section. The pulsed value of the photocurrent is increased to 40 μA to obtain a curve similar to the transient response of the PMOS load device. The response curve shows a more gradual rise time, but a faster fall time than the PMOS load. However, the initial rate of change in V_L is much faster for the NMOS device. Both of the rise times correspond to exponential curves with time constants proportional to the channel resistance of the load device.

4.3 Saturated NMOS Transistor Load

As shown in Fig. 4-8, an n-channel transistor with the gate and drain tied together forms a saturated load device for the detector. The saturation condition of $V_{DS} > V_{GS} - V_{Tp}$ is satisfied since $V_{DS} = V_{GS}$ for all values of drain-source voltage. Under dark conditions the reverse current of the photodiode is too small to sustain the threshold voltage at the gate

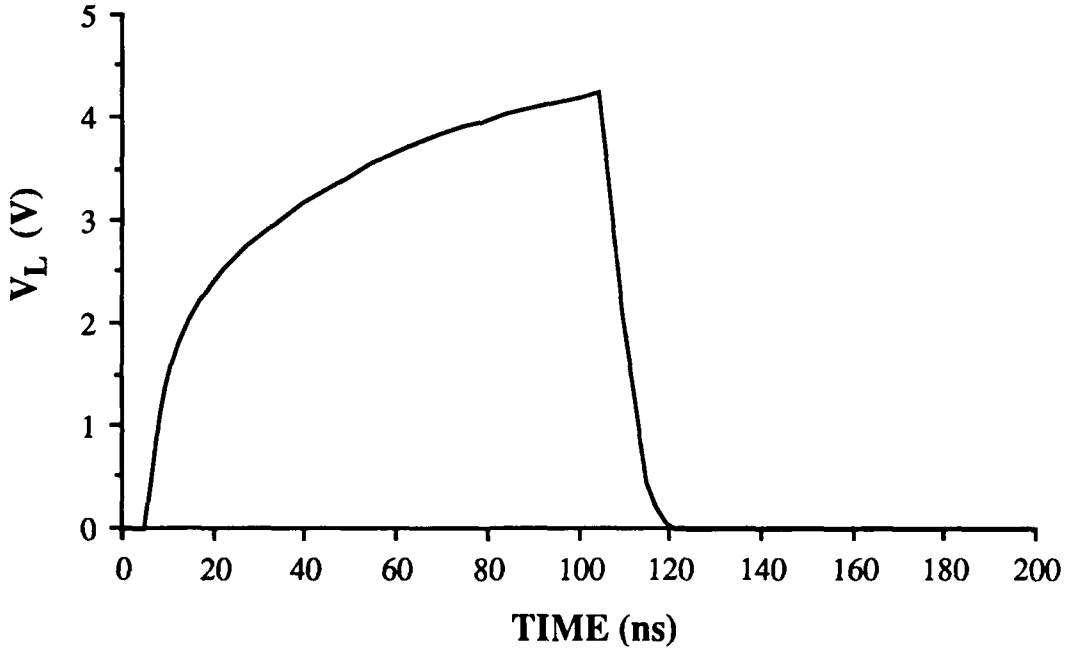


Figure 4-7. Transient Response of the Detector and Nonsaturated NMOS Load.

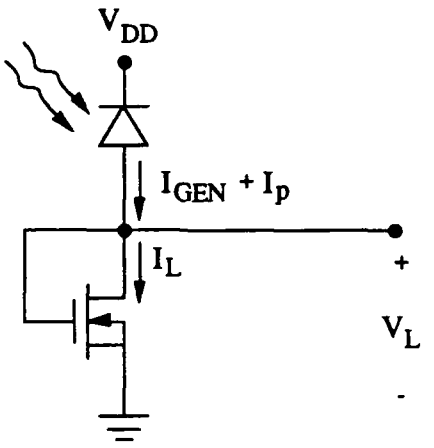


Figure 4-8. Photodiode with a Saturated NMOS Transistor Load.

of the NMOS transistor. The gate voltage drops to the point where the dark current of the diode is approximately equal to the sum of the subthreshold leakage current of the channel and the leakage current into the substrate from the drain n^+ implant. Since the dark voltage of the gate is less than the threshold, the transistor remains in the cutoff mode of operation until the photocurrent charges the gate capacitance to V_{Tp}.

Simulation and experimental results gave significantly different values for V_L under dark conditions. The SPICE simulation gives $V_L = 0.19$ volts when $I_P = 0$. Experimental results for a 50 μm x 50 μm detector and $(W/L)_n = 3/40$ show $V_L = 0.673$ volts with the room lights off and $V_L = 0.96$ volts with the lights on. The difference in experimental results is due to the response of the detector to unfocused room light. In a later section of this chapter, the difference between simulation and experimental results is addressed by the use of empirical data to adjust SPICE model parameters.

As indicated by the transient response shown in Fig. 4-9, the saturated NMOS transistor circuit has the advantage of a high resistance load over the full range of values for V_L. For this simulation, the photocurrent has a pulsed value of 40 μA. Figure 4-10 gives

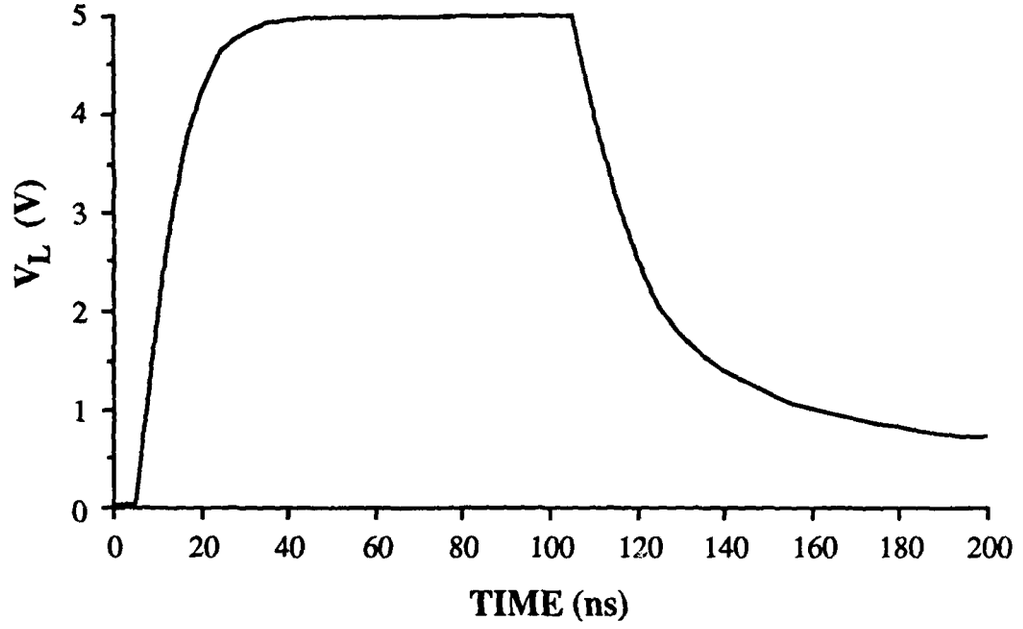


Figure 4-9. Transient Response of the Detector and Saturated NMOS Load.

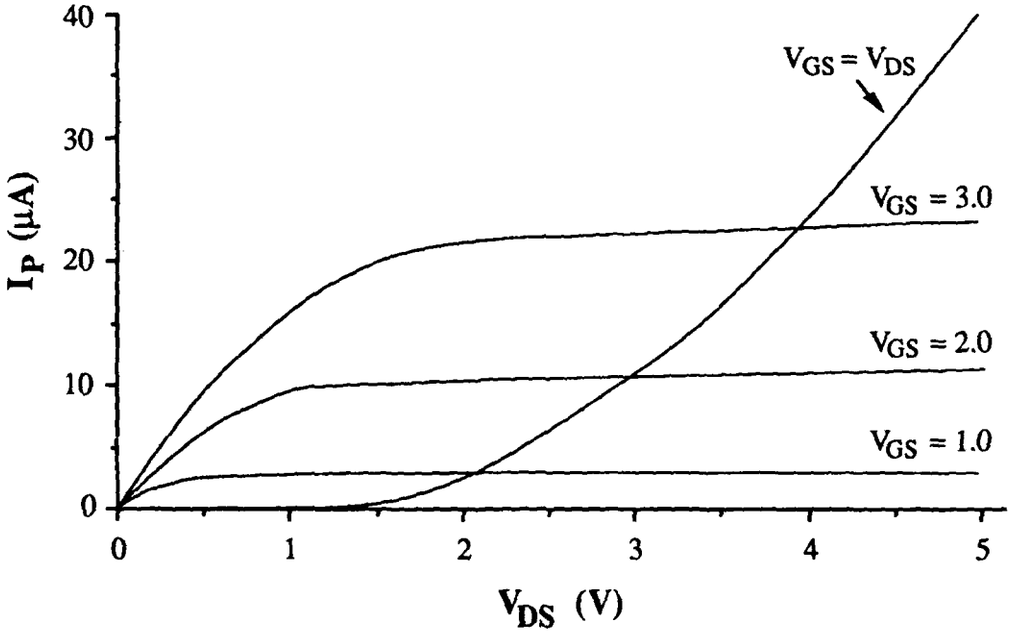


Figure 4-10. Drain Characteristics for a Saturated NMOS Detector Load.

the parabolic curve for $V_{GS} = V_{DS}$, as well as the basic drain characteristics for several values of gate voltage. As the drain-source voltage and gate voltage increase, the channel resistance decreases slightly since the device current-voltage curve has a parabolic shape. For a given drain current the drain voltage is larger for this device than for the nonsaturated NMOS transistor. However, the transient response is slowed by the large gate capacitance that must be charged at the same time as the drain capacitance. Figure 4-10 shows that a drain current of 10 μA gives 3 volts for V_{DS}. However, if I_P is reduced to that value, the transient response is extremely slow due to the large capacitance that must be charged by a small current.

4.4 Cutoff NMOS Transistor Load

Another variation of the NMOS load is shown in Fig.4-11. The gate is simply tied to ground to keep the device in cutoff. This load configuration must be carefully designed such that the sum of the channel leakage current and the reverse current of the n^+ drain implant is greater than the dark current of the photodiode. Generally, the channel of the load device need only be of minimum dimensions since the transistor is in cutoff. The

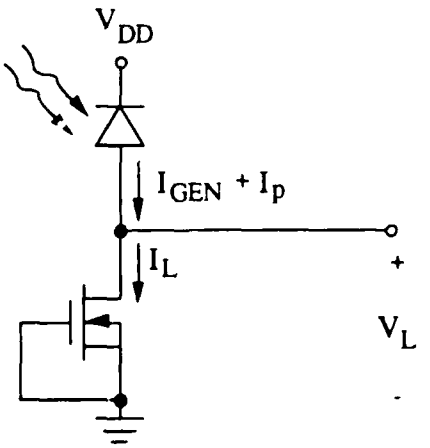


Figure 4-11. Photodiode with a Cutoff NMOS Transistor Load.

the circuit is the size of the drain relative to the size of the detector. Although the drain needs to be large, design flexibility is limited by the effects of a large drain capacitance.

As shown in Fig. 4-12, the rise time of the transient response curve is slow because the capacitance at the drain node of the MOSFET is charged by a photocurrent which is pulsed to only 2 μA. The fall time is also slow since the cutoff MOSFET current must sink the photodiode dark current as well as the discharge current of the load capacitance. Although this circuit may not be useful for transferring data to a static RAM cell, it may be coupled with an electronic or optical reset circuit and function as a dynamic storage node.

The dark output voltage was measured for a 50 μm x 50 μm detector and cutoff NMOS load with $(W/L)_n = 3/20$. The results gave 1.63 volts with the room lights off. Similar results were recorded for a 30 μm x 30 μm detector and $(W/L)_n = 3/3$. These values differ from the simulation results. As described previously, the differences are discussed at the end of this chapter.

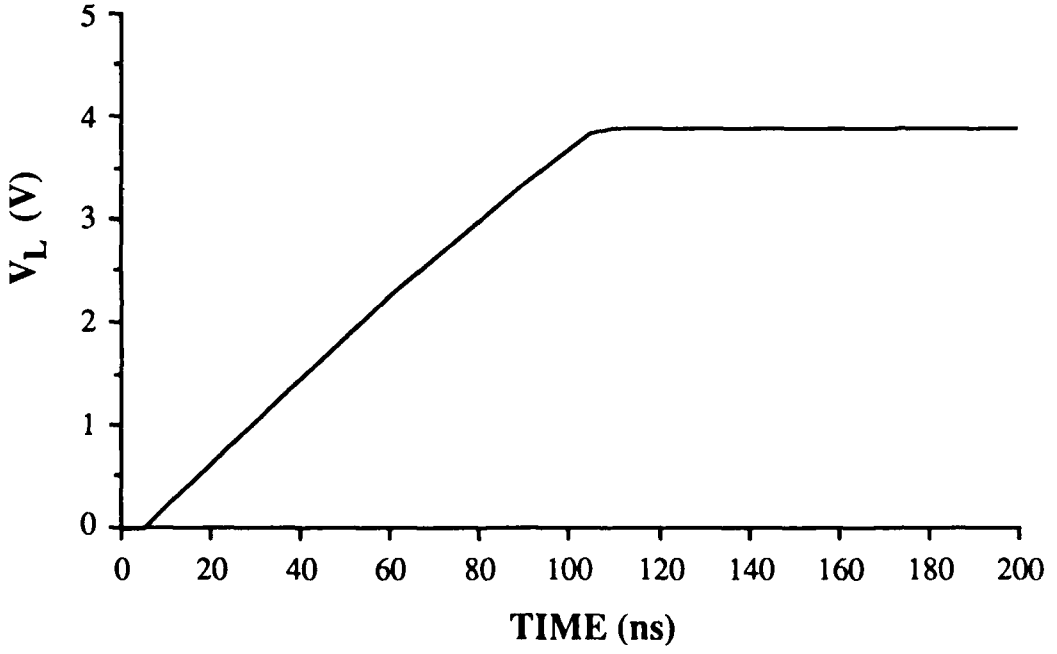


Figure 4-12. Transient Response of the Detector and Cutoff NMOS Load.

4.5 Pull-Down Devices with Gate Bias Circuits

Figure 4-13 shows four examples of load devices which have gates that are biased between ground and V_{DD}. All of these circuits have the common problem of requiring a large area on an integrated circuit chip. Additional static power dissipation may also be a problem when these devices are used in CMOS circuits. The objective of using a gate bias network is to reduce $|V_{GS}|$, which may reduce the required photocurrent and laser power for a desired value of output voltage.

The PMOS load circuit in Fig. 4-13(a) has a saturated p-channel transistor for a gate bias circuit. The primary effect of biasing the gate above ground is to increase the final output voltage. The rate of change of the load voltage is determined by the load capacitance and the charging current. If the value of I_P is unchanged, the response time for this circuit is similar to the circuit in Fig. 4-3.

Biasing the gate above ground also increases the dark output voltage. As described in Section 4.1, the output of the saturated PMOS transistor is approximately 1.3 volts. This becomes the gate voltage of the load transistor, which makes the output of the load device approximately 2.5 volts. Therefore, this configuration can act as an optical input to another circuit which has a high threshold. It may also be useful in creating a new logic scheme, since simultaneous application of light to both diodes drives the output voltage above the supply rail. This can be done with a single light beam when the detectors are jointly located, but separated by at least two depletion layer widths.

The NMOS load circuit in Fig 4-13(b) has a gate bias network consisting of two diodes. The gate voltage is $V_{DD}/2$ when the diodes are identical. When the two bias diodes are not identical, the gate voltage is determined by the relative junction resistance of the devices. The resistance is inversely proportional to device area. In a CMOS fabrication process, at least one of the diodes must be fabricated in a p-well. A p^+n^- diode fabricated in

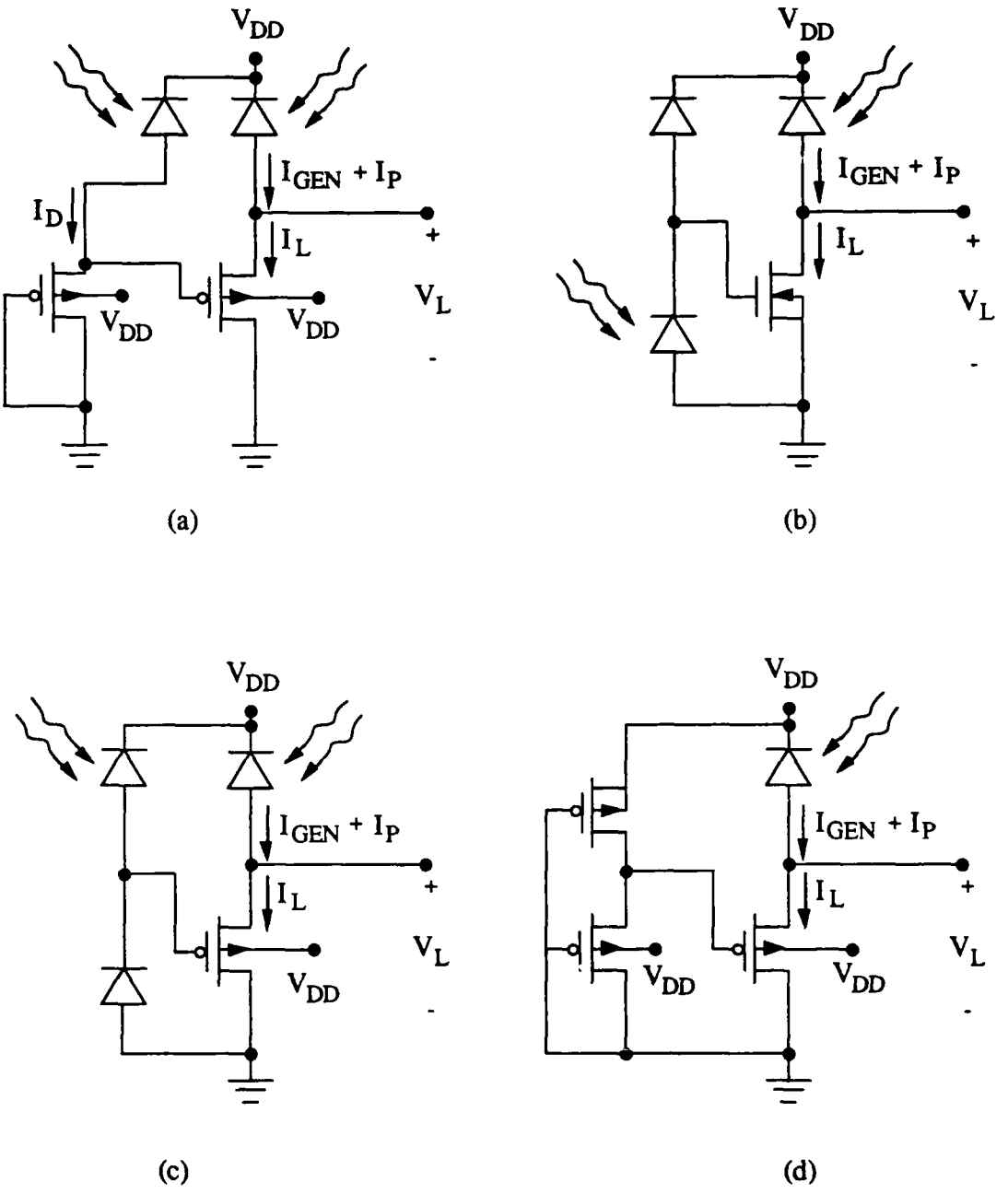


Figure 4-13. Photodiodes with Load Devices and Gate Bias Circuits.

the substrate has no free cathode connection since the substrate and guard ring are connected to the positive supply rail. This device cannot be used for the lower diode in the bias circuit. However, both the upper and lower diodes in Fig. 4-13(b) can be an n^+pn^- device as described in Chapter 3.

Simulation of the circuit in Fig 4-13(b) shows that the photocurrent required to change the output by 4 volts is reduced from 40 μA for the nonsaturated NMOS load in Section 4.2, to approximately 10 μA. Application of light to the two detectors as shown in the figure, reduces the needed photocurrent even further.

The detector and load circuit in Fig. 4-13(c) is similar to the other circuits already discussed in this section. The gate of the PMOS load is biased between ground and the supply rail as in Fig 4-13(a), but with the added flexibility of optically changing the gate voltage as in Fig. 4-14(b). Figure 4-13(d) is an alternate implementation of the circuit in Fig. 4-13(a). Although only a few examples have been shown, an unlimited number of bias arrangements exist. Many of these bias circuits can be used with both PMOS and NMOS loads.

4.6 Pull-up Load Devices

A photodetector with a pull-down load is the primary circuit used for optical data transfer in this thesis. For other applications, it may be useful to start with a high voltage at the detector output and apply a light source to obtain a lower voltage. Many of the devices discussed in this chapter may be used to either pull up or a pull down the voltage. A p-channel transistor used as a pull-up load is shown in Fig. 4-14. The dark output voltage is approximately equal to V_{DD} since a p-channel device passes a strong logic one. The detector must be of a type that has a free n-type region to connect to the drain of the load transistor. This circuit requires more photocurrent per volt change in output than the saturated PMOS pull-down configuration in Fig. 4-3. The increase in current is due to the

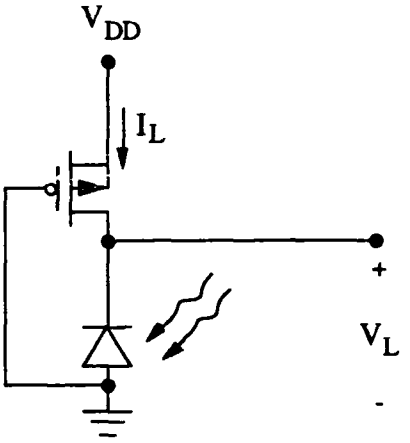


Figure 4-14. Photodetector with a PMOS Pull-Up Load.

difference in gate-source voltage for the circuits. For the same reason, the pull-up circuit recovers to the dark voltage more quickly than the pull-down version. A pull-up load more comparable to the saturated PMOS pull-down is shown in Fig. 4-15. Since $V_{SD} = V_{SG}$, the gate-source voltage starts off at a low value. Due to the increased channel resistance, the circuit requires only 10 μA to obtain the desired simulation results of a 4 volt change in V_L. However, when the photocurrent is off, the output returns to the dark voltage more slowly than the circuit in Fig. 4-14. Simulation results show a dark output of $V_L = 4.5$ V.

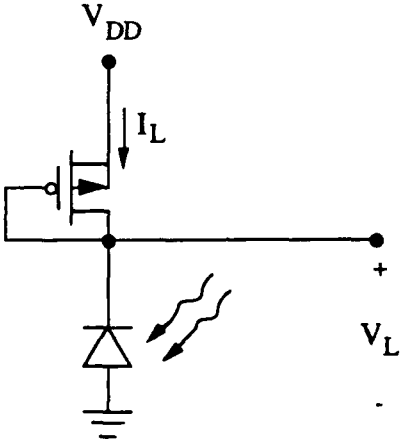


Figure 4-15. Photodetector with a Saturated PMOS Pull-Up Load.

4.7 Experimental Results

This section discusses the experimental measurements for three detector and load circuits. Results are provided for the saturated PMOS load in Fig. 4-3, the nonsaturated NMOS load in Fig. 4-6, and the saturated NMOS load in Fig. 4-8. Measurements were taken using a Helium-Neon laser and the experimental setup described in Appendix B. The experimental results were obtained with the room lights off. For more sensitive circuits, the presence of incoherent light slightly affects the numerical data; however, it has no significant effect on the performance of these circuits when used for optical data transfer.

Figure 4-16 shows the output voltage for the PMOS and saturated NMOS load devices versus incident optical power. The PMOS circuit results are for a 16 μm x 16 μm p^+n^- photodiode and a transistor aspect ratio of $(W/L)_p = 3/31$. An example layout of a detector and load circuit is shown in Fig. 4-18. For the NMOS circuit, the detector and n-channel transistor were fabricated as individual devices on the same chip. External connections were used to obtain the configuration in Fig. 4-8. The p^+n^- detector and transistor dimensions are (50 μm x 50 μm) and 3/40, respectively.

For $V_L > 2$ volts, the NMOS load appears to give better results than the PMOS load. However, the larger detector and longer channel must be taken into consideration. An important feature of the NMOS circuit is that the dark output voltage is large enough to improve the transient response, but still remains below the threshold voltage. This is a desirable characteristic for many applications. A responsivity of 0.178 A/W was given in Chapter 3. When the detector responsivity and device dimensions are considered, the experimental work and simulations in this chapter show similar correlation between output voltage and photocurrent.

Figure 4-17 shows the experimental results for the nonsaturated NMOS detector load. The layout is the same as for the PMOS circuit, except the transistor channel length is

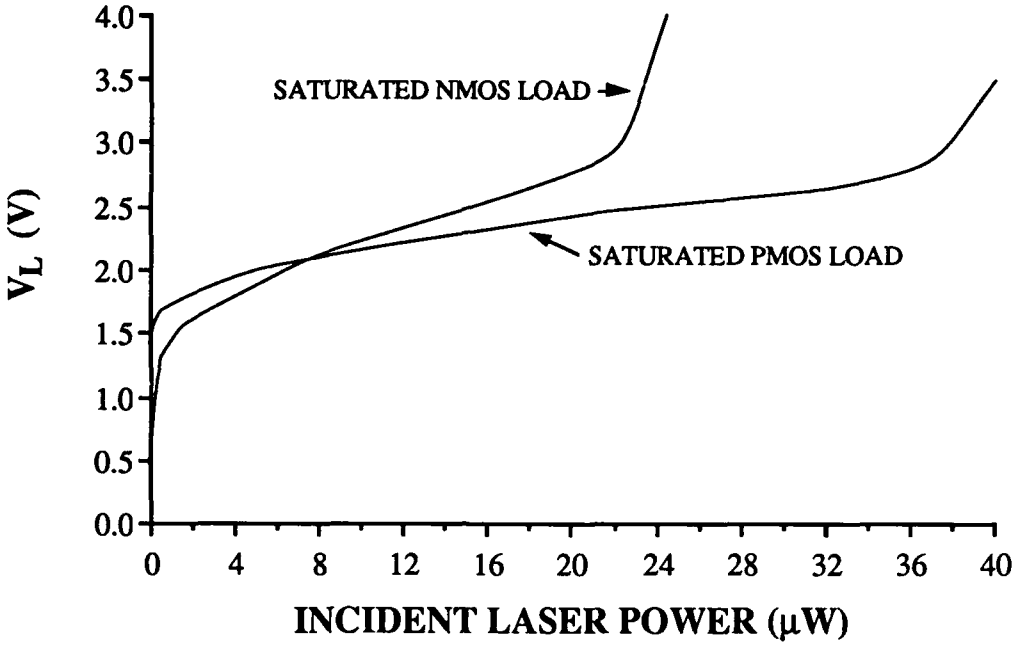


Figure 4-16. Experimental Output Voltage for PMOS and NMOS Detector Loads.

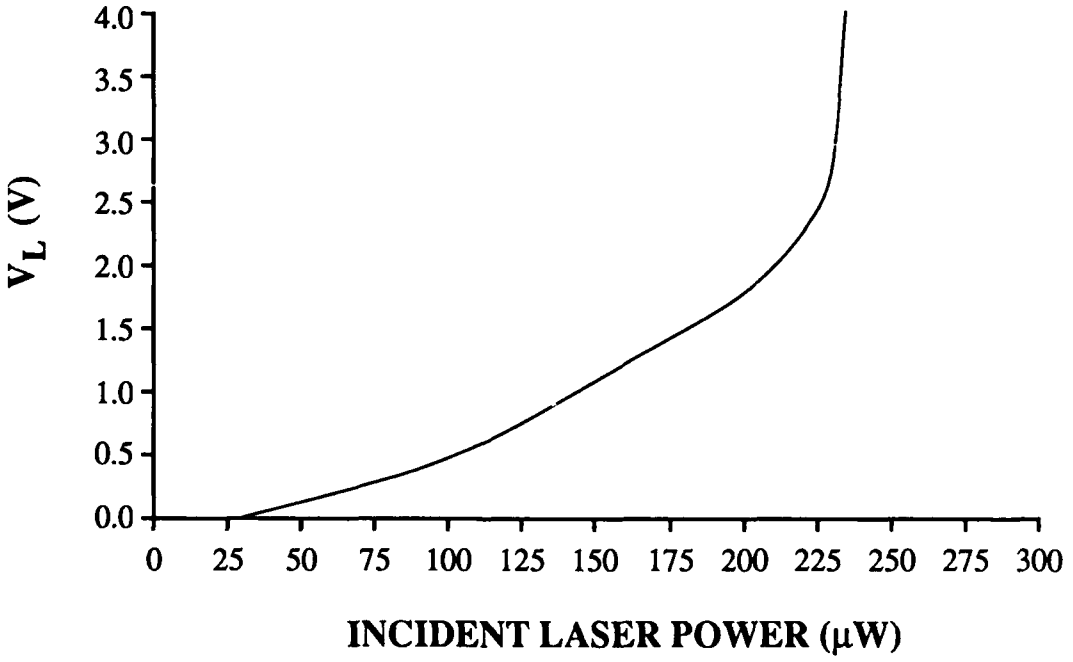


Figure 4-17. Experimental Output Voltage for a Nonsaturated NMOS Detector Load

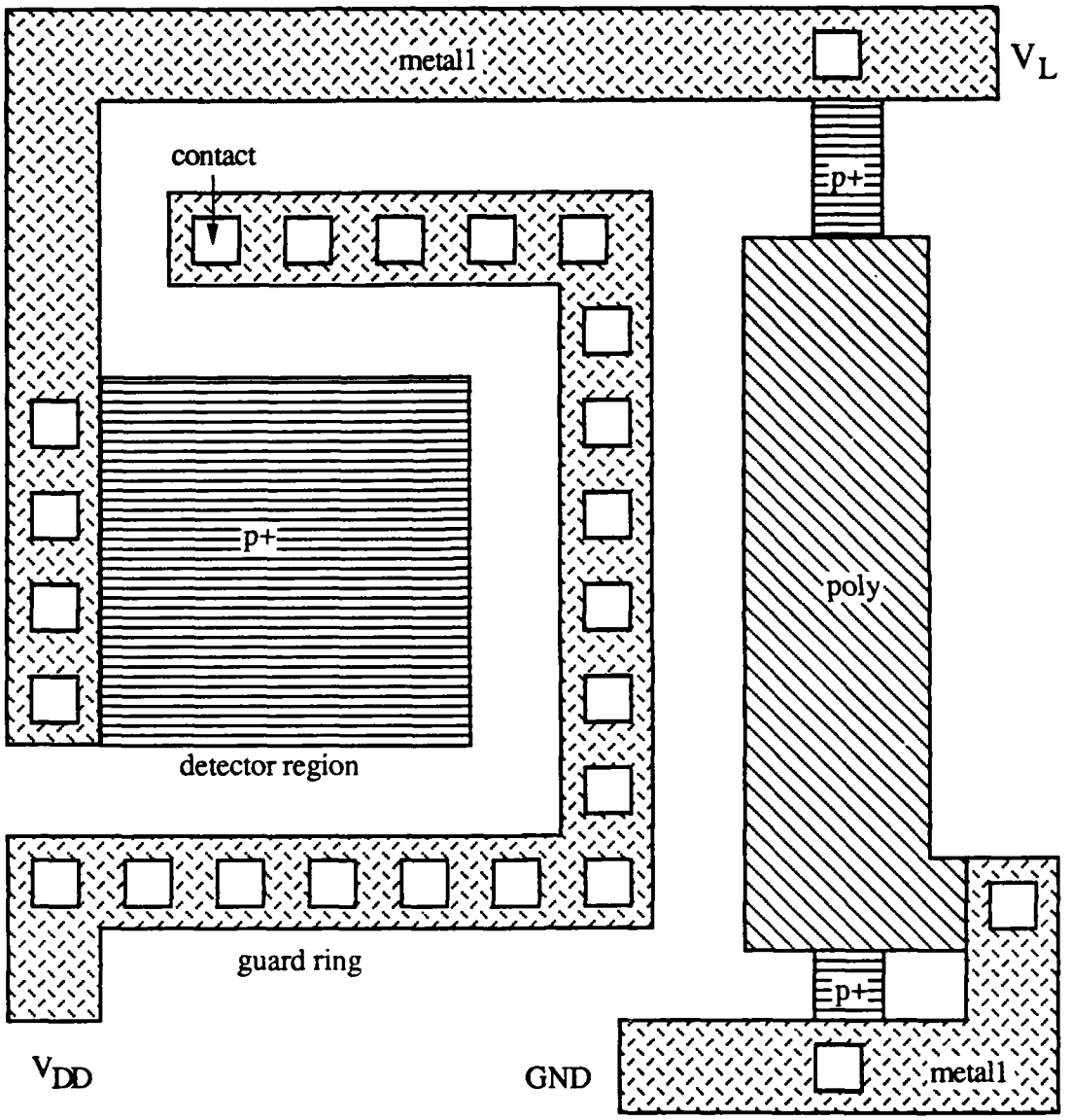


Figure 4-18. Example Layout of a Detector and MOSFET Load.

32 μm. The high laser power eliminates this device from applications that require large detector arrays.

4.8 Empirical Model Parameters

The DC output voltage of the saturated NMOS load circuit discussed in Section 4.3 was determined experimentally to be 0.673 volts. A SPICE simulation of the same circuit gives a much smaller value for V_L when model parameters from Table A-1 are used and the input file reflects the appropriate diode and transistor dimensions. Since the dark output voltage is less than the NMOS device threshold, the transistor is in the cutoff mode. The drain voltage of the MOSFET is determined primarily by the conductance of the channel and the reverse current of the diode.

The channel conductance is determined by V_{GS}, which controls the development of an electron inversion layer underneath the gate oxide [51]. If $V_{GS} > V_{ON}$, the MOSFET is in the active region of operation since strong inversion occurs. This is the point at which the density of the layer of electrons underneath the oxide is equal to the density of holes in the substrate [61]. For a range of positive values of gate voltage less than V_{Tn}, a lower concentration of electrons forms a weak inversion layer. Although the device remains in cutoff, the weak inversion layer allows a small current flows in the channel. The parameter V_{ON} is the gate voltage at the boundary between strong inversion and weak inversion [69].

The DC output voltage from a SPICE simulation depends on how the weak inversion layer current is modeled. The results are primarily determined by the SPICE model parameter NFS. This parameter, called the effective fast surface state density, characterizes the weak inversion current [70] and applies to gate voltages less than V_{ON}, where [69]

$$V_{ON} \simeq V_{Tn} + \frac{nkT}{q} . \tag{4.3}$$

The slope parameter n is given by

$$n = 1 + \frac{q(NFS)}{C_{OX}} + \frac{C_{DEP}}{C_{OX}}, \tag{4.4}$$

where q is the electronic charge, C_{OX} is the oxide gate capacitance, and C_{DEP} is the depletion capacitance. The expression kT/q is the thermal voltage. Two transient response curves are shown in Fig. 4-19 for the saturated NMOS load circuit. Without significantly changing the shape of the curve, an empirical value for NFS was used to match the DC value of V_L to the measured dark output voltage. These results were obtained by reducing NFS from its vendor given value of 2.26×10^{12} cm^{-2} to 4.6×10^{11} cm^{-2}.

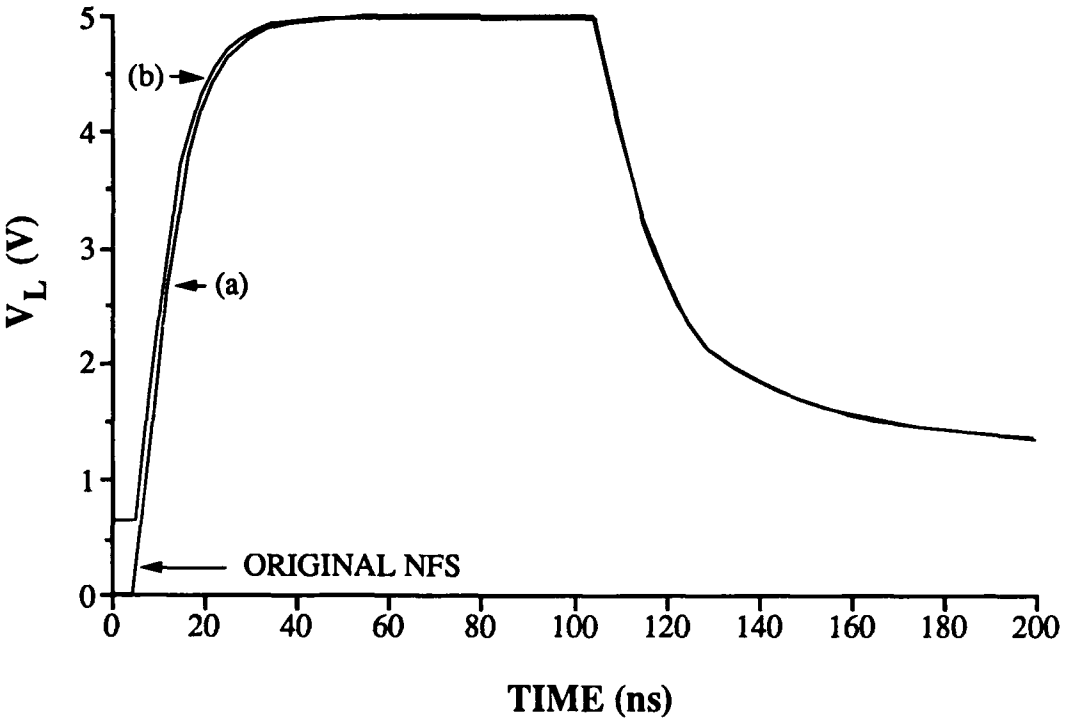


Figure 4-19. Transient Response of the Saturated NMOS Load and Detector. Curves are shown for: (a) the original response, and (b) the response with an adjusted NFS parameter.

4.9 Chapter Summary

Load devices have been added to photodetectors to convert an input optical signal to a DC output voltage. A wide range of simulation and experimental results have been obtained. The best results are provided by the saturated PMOS and NMOS load transistors. In the next chapter, the detector and load circuits are coupled with static CMOS data storage circuits. These complete systems provide detection of optical data, as well as storage of the information for an indefinite period of time.

CHAPTER 5

STORAGE OF OPTICALLY TRANSMITTED DATA

In this chapter optical detection and electronic data storage circuits are combined to obtain integrated systems that detect and store optical data. The detection circuits were described in Chapters 3 and 4, while the CMOS SRAM cells used for data storage were discussed in Chapter 2. For the circuits presented in this chapter, optically transmitted data implies coherent light at wavelengths that can be detected by silicon devices (approximately 0.4 μm to 1.0 μm) and optical signals which have an intensity level high enough to be detected by the light sensitive regions of optoelectronic circuits.

5.1 Review of CMOS SRAM Cell Operations

The static RAM cell discussed in Chapter 2 has six MOSFETs configured as two cross-coupled CMOS inverters and two access transistors. As shown in Fig. 5-1, access transistors T5 and T6 are each connected to a DATA node and a BIT line. The two access devices are controlled by a single word line. Data is written to the cell when the information placed on the BIT lines is transferred to the DATA (D) and NOT DATA ($\overline{D}$) nodes by the access transistors.

As described later in this chapter, the principal operation for optical data transfer is storage of a logic zero in response to the presence of an incident laser beam. The optically written logic zero is similar to the corresponding electrical operation, which occurs when the BIT line (BL) is low and the NOT BIT ($\overline{BL}$) line is either floating or held high , as shown in Fig. 5-1. When the word line is brought high the logic zero is written to the DATA node and a logic one is written to the NOT DATA node. A logic zero may be

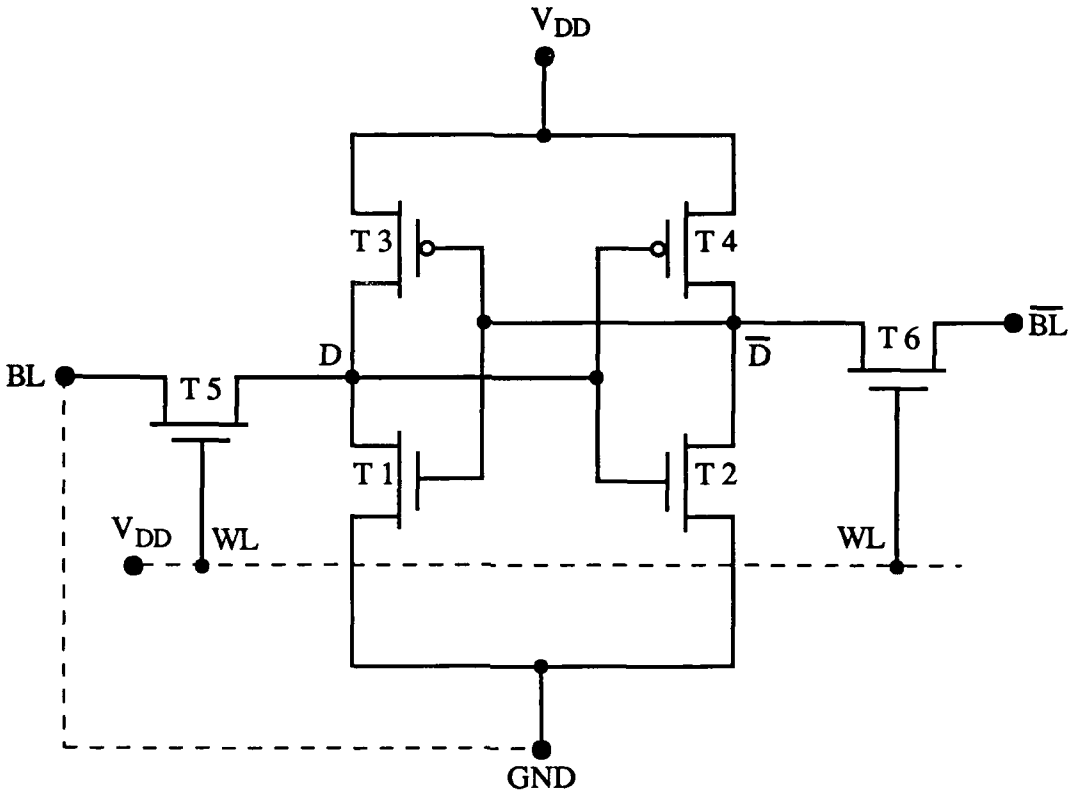


Figure 5-1. CMOS SRAM Cell Electrical Write Operation.

written to the NOT DATA node by reversing the logic pattern placed on the BIT lines and again raising the word line to a logic one. This operation simultaneously writes a one to the DATA node.

5.2 Optical Write Circuit Design

The detection and storage of optically transmitted data is based on the transfer of a logic zero to a storage node using a single bit line principle. Although a logic one may be written directly to a storage node of a CMOS static RAM cell, it is more practical to write a logic zero to the opposite node and force a logic one at the desired location. Using a single BIT line to write a logic one directly to a DATA node is more difficult because the access transistor must provide current to the drain of the NMOS inverter transistor and

simultaneously charge the node capacitance. When a logic zero is stored at the DATA node, a large amount of current is required to raise the drain-source voltage to a logic one level. The problem is aggravated by the inclination to improve the SRAM cell static noise margin by making the access transistors smaller than the NMOS inverter transistors.

The detection and storage circuits presented in this chapter are designed to receive optical input from a holographic ROM. To minimize the complexity of the ROM, the optical circuit controls just one side of each SRAM cell and writes only a logic zero during the detection and storage process. Thus, the presence of laser light stores one bit of data, while the absence of light accounts for its complement. This means that all DATA nodes need to be set to a logic one prior to the selective application of light to the detector circuits within the array.

Optical circuits for writing both a logic zero and a logic one are discussed in this section, despite the difficulty in writing a logic one directly to the storage node of a CMOS SRAM cell. The latter circuits are presented due to their usefulness as inputs to logic circuits and as control elements for numerous other applications.

5.2.1 Optical Circuits for Writing a Logic Zero

A circuit for optically writing a logic zero to the DATA node of a static RAM cell is shown in Fig. 5-2. Several photodetector load devices were discussed in Chapter 4. The saturated PMOS load device is used for this analysis. The MOSFETs are labeled T7 and T8 to distinguish them from the six transistors of the CMOS SRAM cell. Capacitor C_{DATA} represents the storage node for optical data. The operation of the optical write zero (OWZ) circuit in the figure is similar to that of the BIT lines and access transistors of the SRAM cell described in Section 5.1. Transistor T8 functions as an access device with the BIT line end permanently connected to ground. The detector and load form the control circuit for the gate of T8 similar to the word line control of access transistors T5 and T6 in Fig. 5-1.

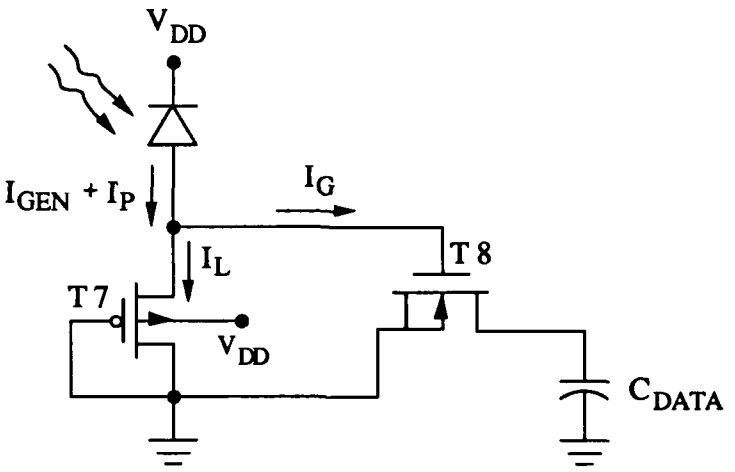


Figure 5-2. Optical Detection Circuit for Writing a Logic Zero.

When light is incident on the detector, the photocurrent increases the source-drain voltage of T7 such that T8 turns on and discharges C_{DATA}. Ignoring channel-length modulation, the source current of T7 is given by [51]

$$I_{Sp} = \frac{\beta_p}{2}\left(V_{SG} + V_{Tp}\right)^2, \tag{5.1}$$

where

$$\beta_p = k_p'\left(\frac{W}{L}\right)_p \tag{5.2}$$

and

$$V_{Tp} = V_{TOp} - \gamma_p\left(\sqrt{V_{BSp} + 2|\phi_F|} - \sqrt{2|\phi_F|}\right). \tag{5.3}$$

In equation (5.2), the symbols β_p and k_p' are the p-channel transistor transconductance parameter and the process transconductance parameter, respectively. Other symbols are as defined in Chapters 2 and 4. The effects of body bias are included in this circuit to account for the independent source and bulk voltages.

Using $k'_p = 21.8 \times 10^{-6}$ A/V^2 and the other model parameters in Table A-1, a plot of equation (5.1) is shown in Fig. 5-3 with $V_{SG} = V_{SD}$ and the transistor aspect ratio as a parameter. Channel-length modulation and body bias effects are included in the determination of source current I_{Sp}. Under static illumination, the photocurrent I_P is approximately equal to I_{Sp}. Thus, the plot gives the approximate static photocurrent needed to obtain a particular source voltage for T7 or gate voltage for T8. As shown, the current may be reduced by increasing the channel length of transistor T7. The length of the load device channel is constrained by the desired discharge rate of the gate capacitance of T8. When the light source is turned off, T7 must sink the current from the capacitance at its source node as well as the dark current of the photodiode. The increased resistance of a longer channel will cause the source of T7 to more slowly drop to the dark output voltage. Thus, the fall time of the transient response curve may be longer than the rise time.

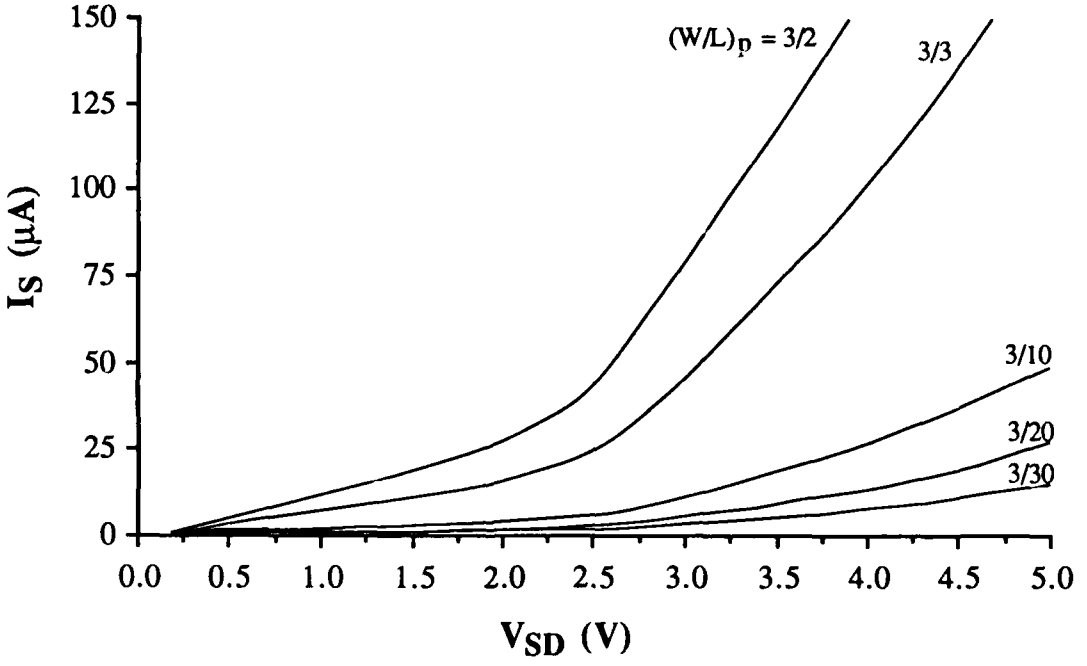


Figure 5-3. Source Current for a Saturated PMOS Load Transistor. The plot is for $V_G = 0$ and $V_{SD} = V_{SG}$.

Transistor T7 controls the gate voltage of T8. The initial value of the drain voltage of T8 is approximately equal to V_{DD}. This places the transistor is in the saturation region of operation at the start of the optical write process. The drain current is expressed as [51]

$$I_{Dn} = \frac{\beta_n}{2}(V_{GS} - V_{TOn})^2(1 + \lambda_n V_{DS}) \tag{5.4}$$

where $\beta_n = k'_n(W/L)_n$ is the n-channel MOSFET transconductance parameter and λ_n = 0.0237 V^{-1} is the channel-length modulation factor. A plot of the gate voltage versus the drain current of T8 is shown in Fig. 5-4 for $k'_n = 55.1 \times 10^{-6}$ A/V^2 and $V_{TOn} = 1.0$ V. Although I_D is larger for increased channel widths, T8 may need to be a minimum geometry device when the total photocurrent is small (e.g. less than a few microamperes). In this case, the slowly rising gate voltage may cause the drain current of a larger T8 to be

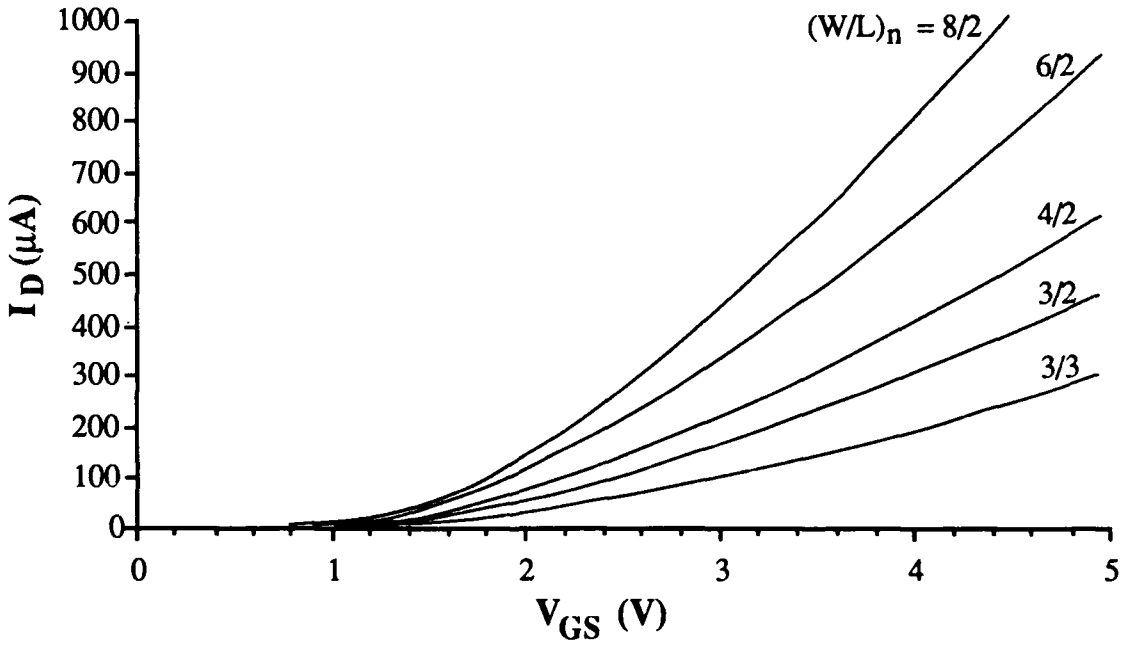


Figure 5-4. Drain Current of Transistor T8 versus Gate Voltage.

less than that of a minimum geometry device at a given time point during the transient response of the circuit. The advantage of increasing the channel width is then offset by the slower response time. The result is that although a larger transistor provides more drain current at each level of gate voltage, the smaller device may write a logic zero to the cell more quickly. The transient response of the optical detection and storage cell to a photonic input is addressed in Section 5.5.2.

An important parameter is the output drain current of NMOS transistor T8 when a steady-state photocurrent flows. The static output current for a given input photocurrent is primarily determined by the relative aspect ratios of T7 and T8. The SPICE simulation in Fig. 5-5 shows the drain current of T8 versus the source current of T7 for $(W/L)_p = 3/30$ and $(W/L)_n = 4/2$. Since I_G in Fig. 5-2 is assumed to be zero (or the transient response of the circuit is ignored), the photocurrent is approximately equal to the source current of T7. The current amplification factor, which may be extracted from the graph, quickly rises to a

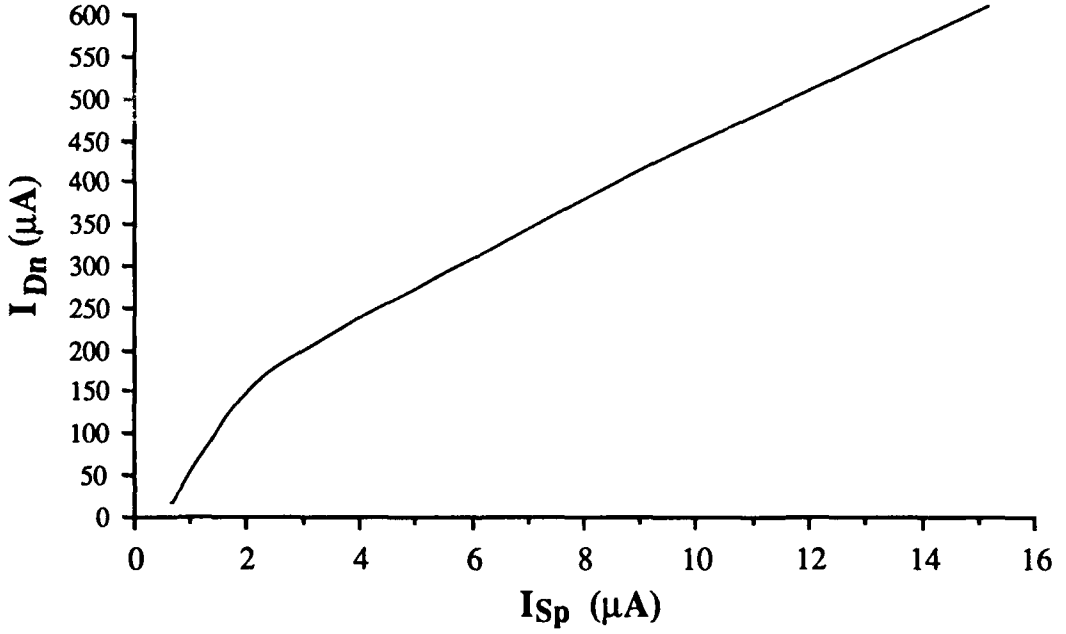


Figure 5-5. Source Current of Transistor T7 versus Drain Current of T8. The simulation results are for $(W/L)_p = 3/30$ and $(W/L)_n = 4/2$.

peak value of 72 and then gradually decreases to about 40. In designing the OWZ circuit, consideration is given to this amplification factor as well as the total current necessary for writing a logic zero. The gate capacitance of transistor T8 and the channel length of T7 are also considered due to the effect they have on the temporal response of the circuit.

An approximate relationship between the drain current of T8 and the input photocurrent can be determined from the MOSFET circuit equations. For steady-state conditions when $I_P \approx I_{Sp}$, the detector and load circuit output voltage V_{SGp} can be determined from equation (5.1). Neglecting channel-length modulation, the PMOS transistor gate voltage is found to be

$$V_{SGp} = \sqrt{\frac{2I_P}{\beta_p}} - V_{Tp}\,, \tag{5.5}$$

which is only valid for $V_{SGp} > |V_{Tp}|$ with body-bias effects included. Since V_{SGp} is equal to V_{GS} for transistor T8, substitution of equation (5.5) into equation (5.4) gives

$$I_{Dn} = \frac{\beta_n}{2}\left(\sqrt{\frac{2I_P}{\beta_p}} - V_{Tp} - V_{Tn}\right)^2 \tag{5.6}$$

where the channel-length modulation effect on the NMOS transistor has been neglected. Equation (5.6) is valid while T8 is in the saturation region or $V_{DS} \geq V_{GS} - V_{Tn}$. Using this expression and equation (5.4), the drain current of T8 is plotted as a function of I_P in Fig. 5-6. Device parameter values are the same as those used previously in this chapter. This graph indicates the steady-state detector output current when the minimum required current for T8 is known. These results are consistent with the simulation plot in Fig. 5-5.

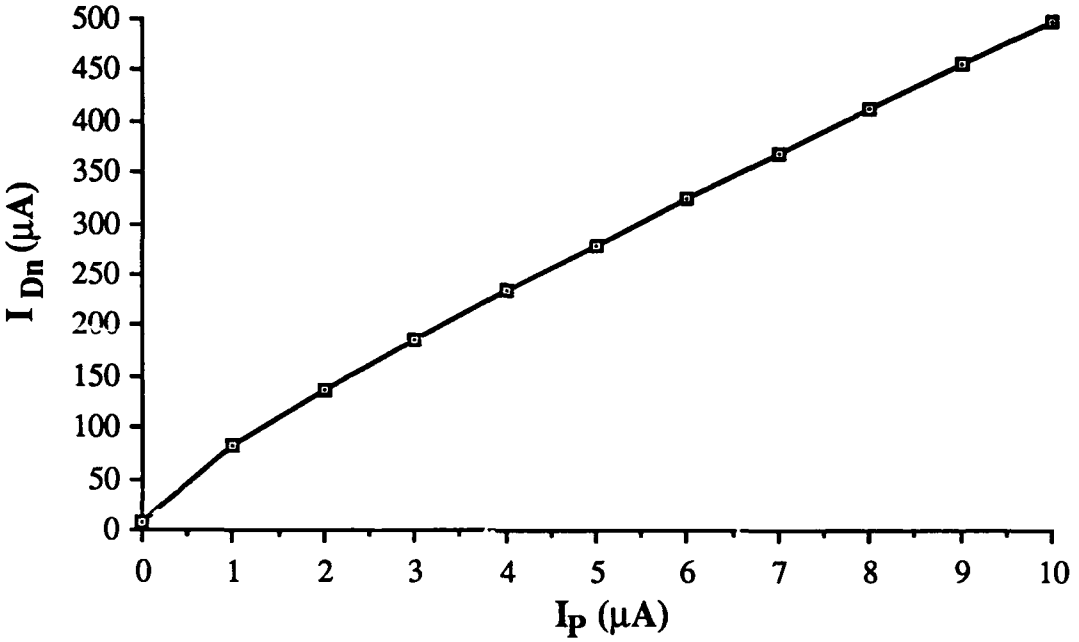
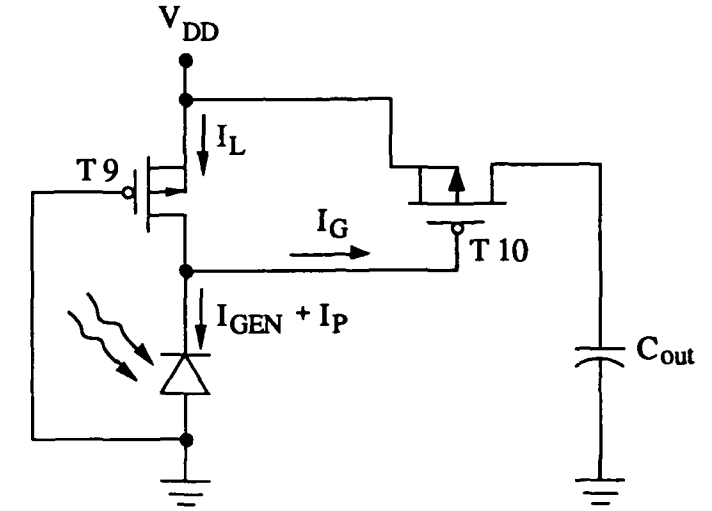


Figure 5-6. Drain Current of T8 versus Photocurrent Under Static Conditions. $(W/L)_n = 4/2$ and $(W/L)_p = 3/30$.

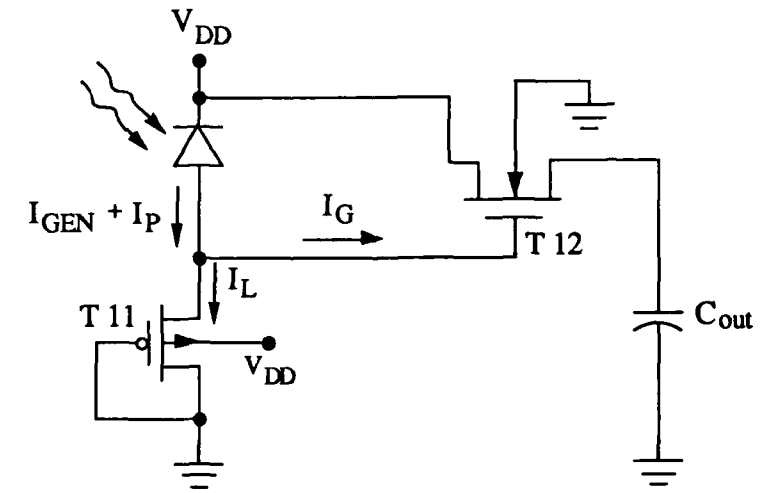
5.2.2 Optical Circuits for Writing a Logic One

An optical circuit may be designed to pass a logic one in a manner similar to the transfer of a logic zero from a BIT line to a DATA node. Figure 5-7 shows two circuits that may be used for this purpose. Although only two load devices are shown, many other possibilities were suggested in Chapter 4. In Fig. 5-7(a), PMOS transistor T9 is biased in the linear region of operation. When $I_p = 0$, the source-drain voltage is approximately zero and the dark output voltage of the detector is near V_{DD} since the load device passes an undegraded logic one. As the photocurrent increases, the drain of T9 is pulled down, while the gate capacitance of T10 discharges. This turns on T10, which passes a logic one and sources current to an external load.

The circuit in Fig 5-7(b) is the same as the OWZ circuit presented in Section 5.2.1, except one end of the pass transistor is connected to V_{DD} instead of ground. The photocurrent charges the gate capacitance of T12 such that the device turns on and passes a



(a)



(b)

Figure 5-7. Circuits for Optically Writing a Logic Zero. (a) PMOS transistor pull-up. (b) PMOS transistor pull-down.

degraded logic one. With an NMOS transistor is used as the pass transistor, this circuit provides more current to the load than the circuit in Fig. 5-7(a) when device geometries are similar. However, since both PMOS and NMOS devices are used in Fig. 5-7(b), additional layout space is needed for separation between the PMOS transistor and the p-well. An all NMOS version of the same circuit is shown in Fig. 5-8. Both T13 and T14 can be fabricated in the same p-well diffusion region of a chip. Simulation and experimental results were given in Chapter 4 for the saturated NMOS load transistor used in this circuit. The operation and photocurrent requirements are similar to that of the circuit in Fig. 5-7(b), except the load device is in cutoff under dark conditions.

5.2.3 Experimental Results

Experimental values for the drain current of an n-channel MOSFET as a function of gate voltage are shown in Fig. 5-9. To provide a reference for experimental results, the SPICE simulation values for the same device are also shown on the graph. The transistor used for experimentation was fabricated as a separate device on a chip with other optoelectronic circuits. The channel aspect ratio is $(W/L)_n = 4/2$ for the experiment and the

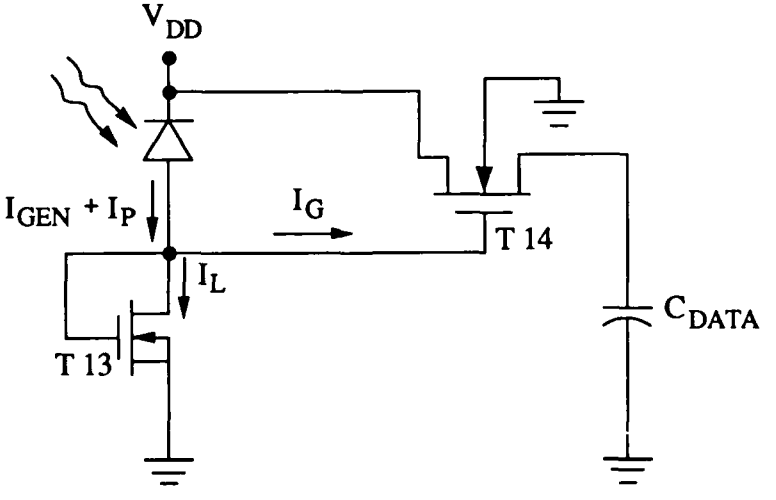


Figure 5-8. NMOS Circuit for Optically Writing a Logic One.

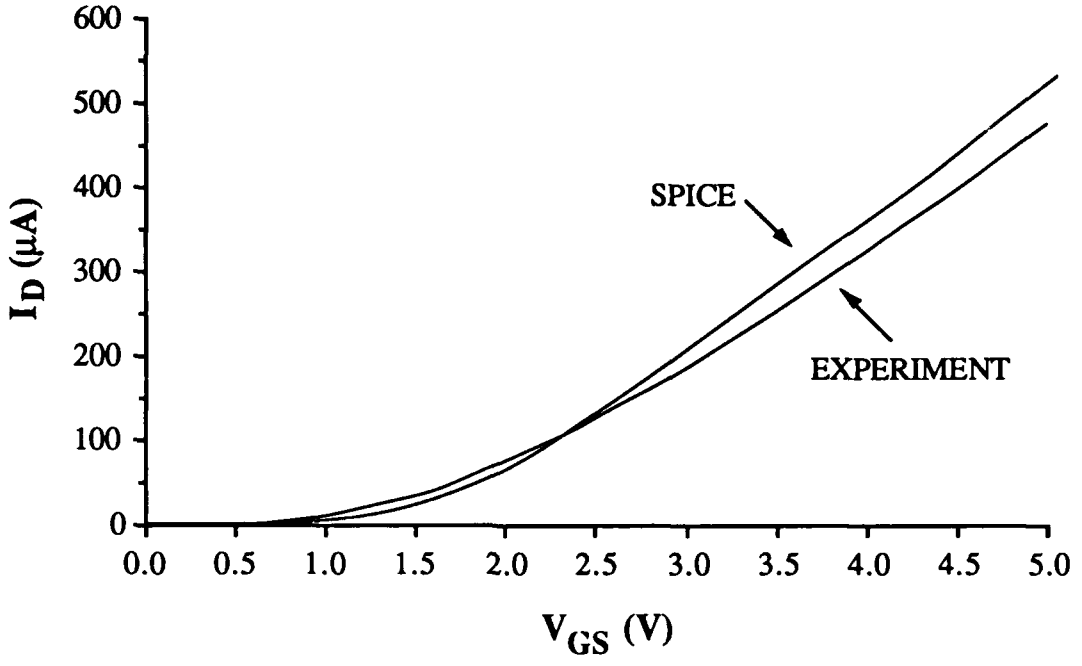


Figure 5-9. Experimental NMOS Transistor Drain Current versus Gate Voltage. Simulation results are also shown for V_{DS} = 5 volts.

simulation. A simple procedure based on two power supplies was used to obtain the experimental results. One power supply was connected to a variable resistor which controlled the gate voltage of the transistor. The other power supply was connected to the drain of the device through a 1.5 kΩ resistor. A small resistor was used to maintain a large value for V_{DS}, which is representative of the initial conditions for the optically written logic zero and the conditions for the simulation. The drain current was measured via the voltage drop across the 1.5 kΩ resistor. In Fig. 5-9, the agreement between the simulation and experimental results for $V_{GS} < 3$ V implies that the pass transistor current necessary to optically write a logic zero can be estimated from a combination of experimental and simulation data provided here and in Chapter 4. Generally, the logic zero is written when the gate voltage of T8 is less than 3 volts. Those results are given in a later section of this chapter.

5.3 Optical Detection and Storage Cell

In this section, the SRAM cells presented in Chapter 2 are combined with the optical write circuits in Section 5.2. The resulting optical detection and storage cells have electrical read and write functions as well as the ability to detect and store data contained in an incident light beam of appropriate wavelength and intensity. Most cells presented in this section contain eight MOSFETs and one photodiode, with six of the transistors pertaining to the standard CMOS SRAM cell.

5.3.1 Detection and Storage of a Logic Zero

A cell for the detection and storage of an optically transmitted logic zero is shown in Fig. 5-10. Aspect ratios for the six transistors of the basic SRAM cell are selected based

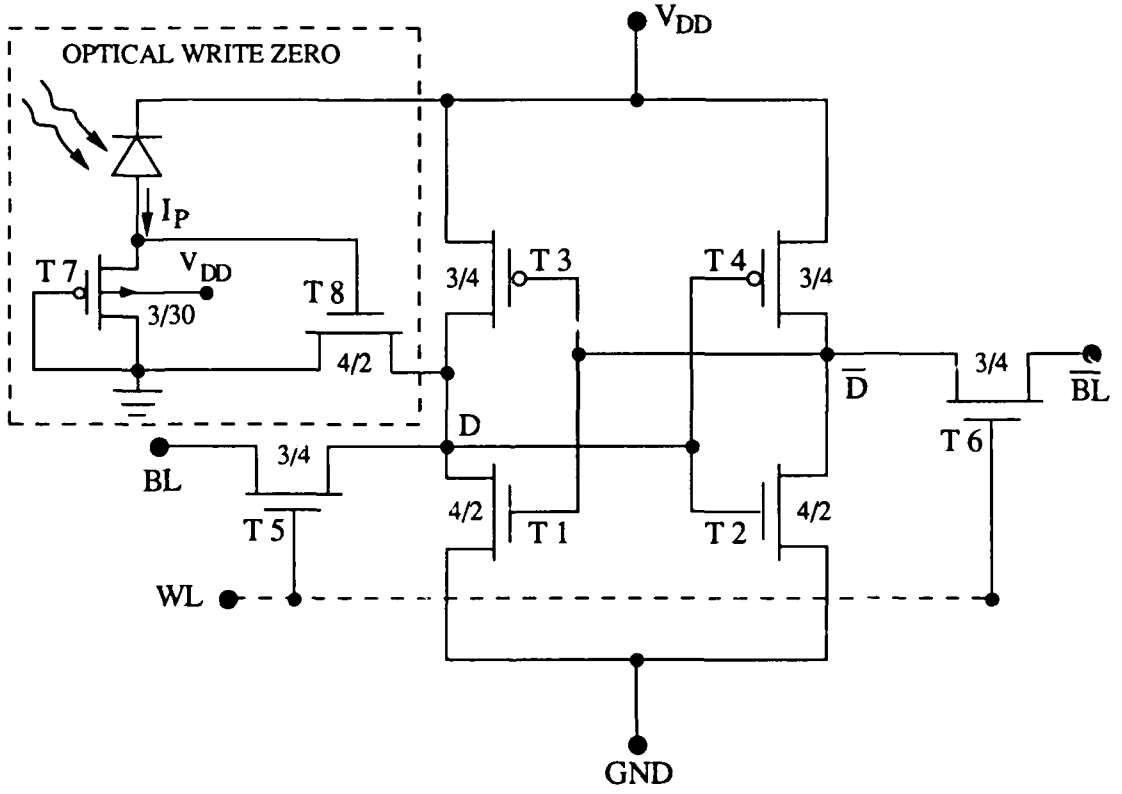


Figure 5-10. Circuit for Detection and Storage of an Optically Transmitted Logic Zero.

on the design information provided in Chapter 2. The optical portion of the cell is designed from data provided in Chapter 4.

As discussed in Section 5.2, the OWZ circuit in Fig. 5-10 writes a logic zero to the cell in the same manner as the electrical operation of the word line and access transistor. For the optical circuit, the photocurrent raises the source-drain voltage of transistor T7 and the gate voltage of T8. As the gate voltage increases, transistor T8 sinks a portion of the current from T3 and discharges the capacitance at the DATA node. The SPICE circuit simulator and the model parameters in Table A-1 were used to obtain the transient response curve for the optically written logic zero as shown in Fig. 5-11. The parameters, including $k'_n = 55.1 \times 10^{-6}$ A/V^2 and $k'_p = 21.8 \times 10^{-6}$ A/V^2, are average values extracted from MOSIS fabrication runs over the eight month period from July 1989 to February 1990. The photocurrent was simulated by a current source in parallel with the diode. As shown in Fig. 5-12, a pulse having rise and fall times of 1 ns and a peak value of 10 μA was

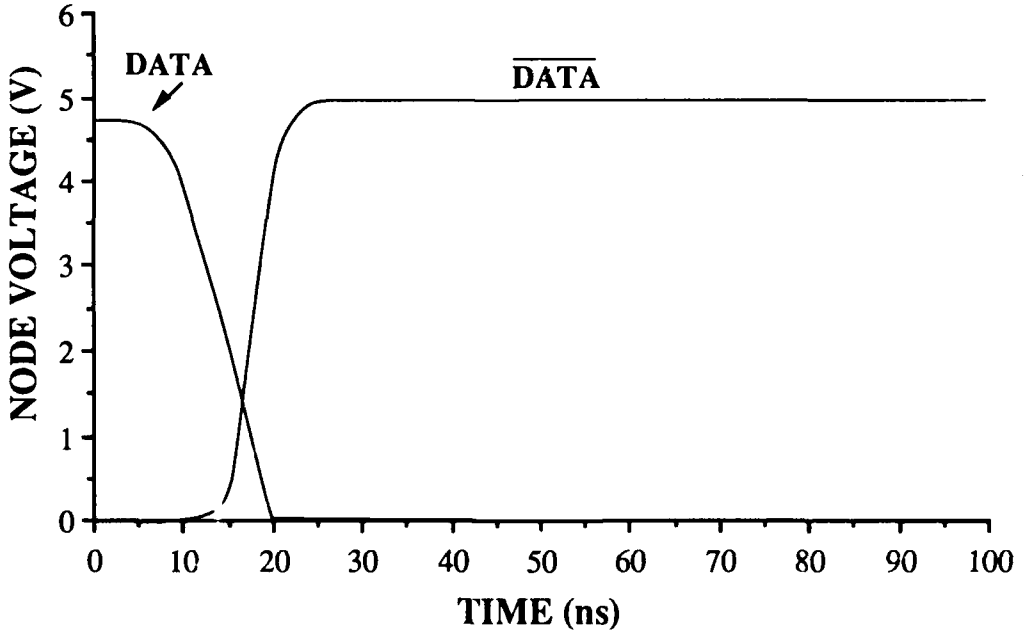


Figure 5-11. Transient Response Curve for Optically Written Logic Zero.

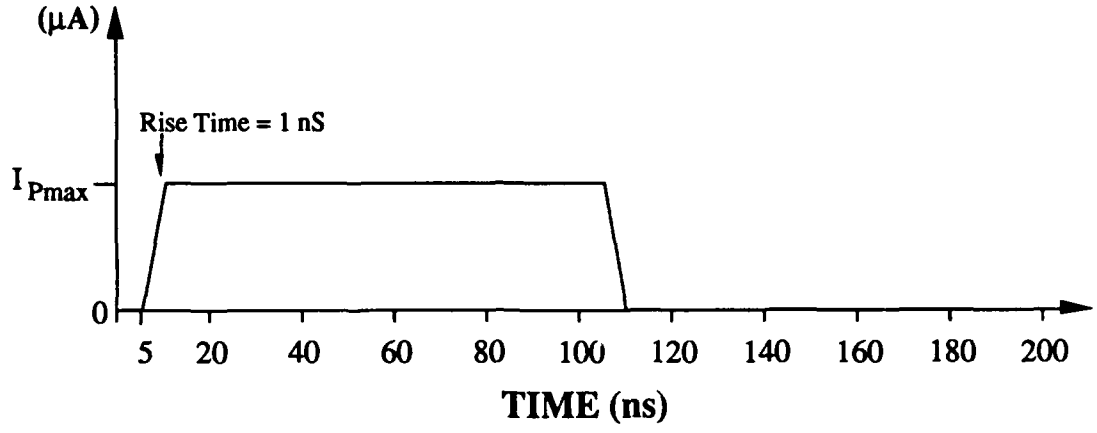


Figure 5-12. Input Photocurrent for Optical Write Zero Simulations.

arbitrarily selected. The short rise time implies that carrier diffusion from the substrate to the depletion layer of the detector is ignored. The primary purpose of the simulations in this section is to demonstrate the operation of the optical portion of the cell. An estimate of the actual transient behavior is given in Section 5.5.

The results in Fig. 5-11 show the transfer of a logic zero to the DATA node of the cell and a logic one to the NOT DATA node in approximately 20 ns. Figure 5-13 shows the same transitions as a function of the gate voltage of transistor T8. The optical write process is complete when V_{GS} is approximately 2.3 volts. For the optically written logic zero, the gate voltage at which the transition occurs is determined by the amount of current T8 must sink to discharge the capacitance at the DATA node. Thus, the required value of V_{GS} is independent of I_P. The theoretical value for the detector output then becomes 2.3 volts for the transfer of optical data to the cell.

From the experimental and simulation data in Fig. 5-9, the theoretical V_{GS} implies transistor T8 must sink at least 75-80 μA to pass a zero to the DATA node. The projected laser power required for optical data transfer can be extracted from Fig. 4-16. For an output of 2.3 volts, the detector with a saturated PMOS load requires an optical input of

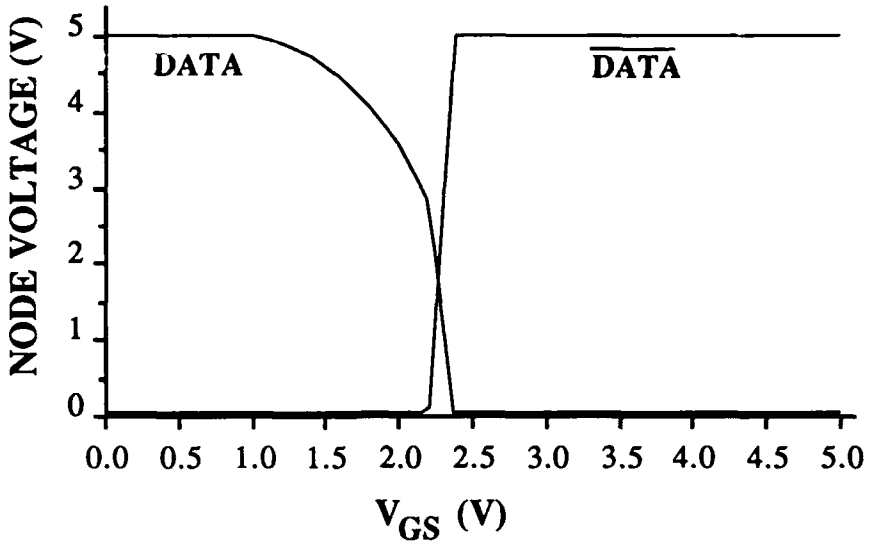


Figure 5-13. DATA Node Voltage as a Function of Transistor T8 Gate Voltage.

8-12 μW. This assumes the laser light is contained within the boundaries of the photodetector. When the beam spot radius is 15 μm and the detector dimensions are 16 μm x 16 μm, the simple ratio of areas in equation (3.4) reduces the required incident optical power to 2.9-4-3 μW. These values are consistent with the experimental results in Section 5.3.3.

5.3.2 Optical Detection and Storage Cell Layout

The layout for a single optical detection and storage cell is shown in Fig. 5-14. The design rules for the layout are based on a CMOS p-well fabrication process with two metal layers and one or two polysilicon layers. The second polysilicon layer was ignored. Scalable CMOS rules for a 2 μm (lambda=1.0) process were used. The minimum channel width for MOSFETs was 3 μm. Additional information on the layout and fabrication procedure is given in Appendix A.

The cell area was not minimized since the total dimensions needed to be 100 μm x 100 μm to be compatible with the optical input signals. The light sensitive region measures

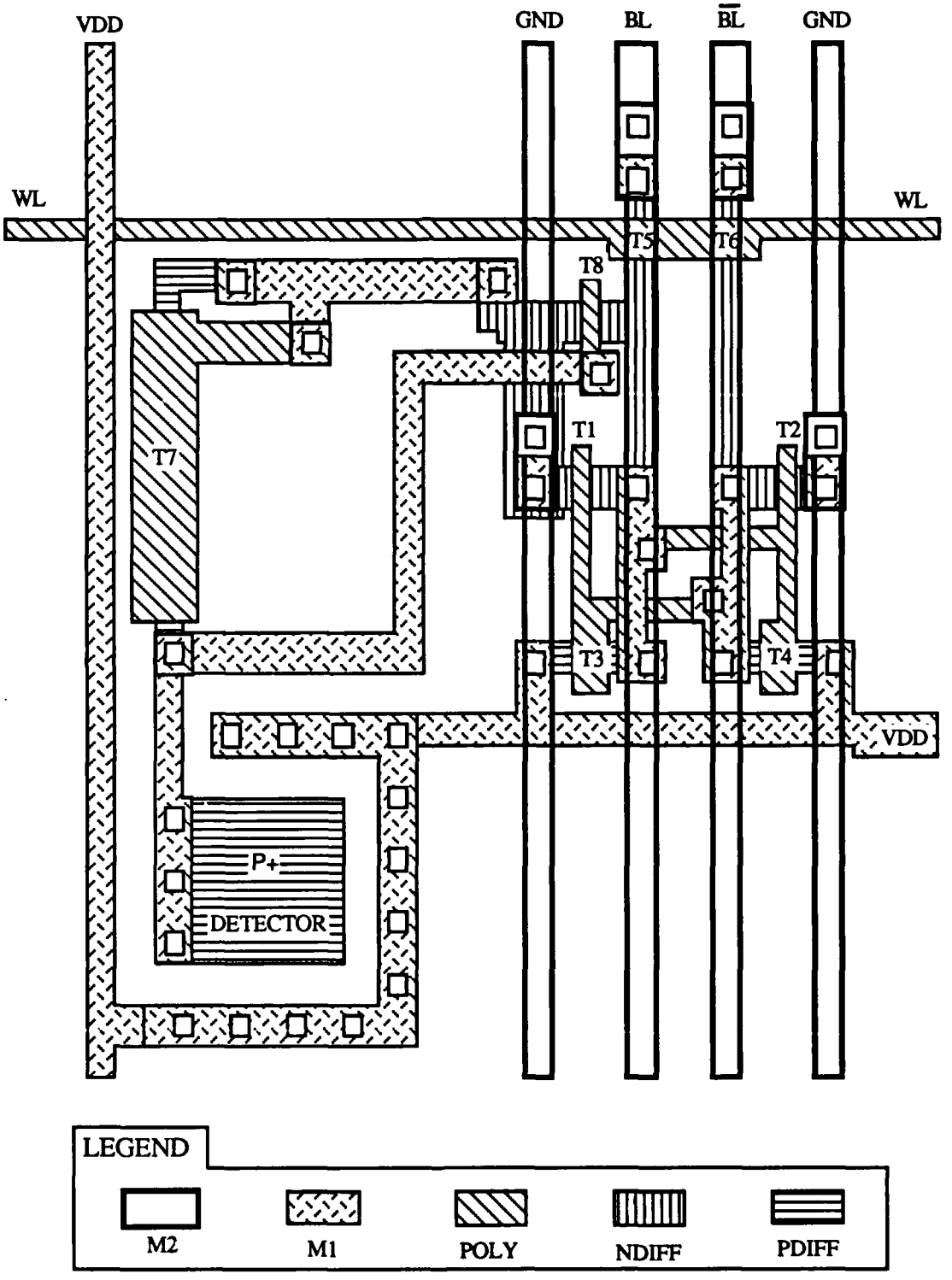


Figure 5-14. Layout of an Optical Detection and Storage Cell.

16 μm x 16 μm and is protected on three sides by a guard ring made up of a chain of substrate contacts. The BIT line, NOT BIT line, and ground run vertically in the metal2 layer. A single word line runs horizontally in polysilicon. The supply bus runs across the guard ring and in both directions in the metal1 layer. Well and substrate contacts are not shown, except for the guard ring. Generally, contacts for biasing the n^- substrate and p-wells are located adjacent to the source contacts for each of the PMOS and NMOS transistors, respectively.

A photograph of a test cell is shown in Fig. 5-15. In this circuit the detector was placed approximately 100 μm from the RAM cell. This type of layout does not apply to the cells iterated to form an array. The configuration in Fig. 5-15 was used for initial verification of the optical data transfer concept and to determine if reductions in crosstalk significantly improved the optical performance of the cell. No crosstalk problems were encountered in this cell or in the cells fabricated according to the layout in Fig. 5-14. Several other cells with different detector dimensions and transistor aspect ratios were fabricated and tested.

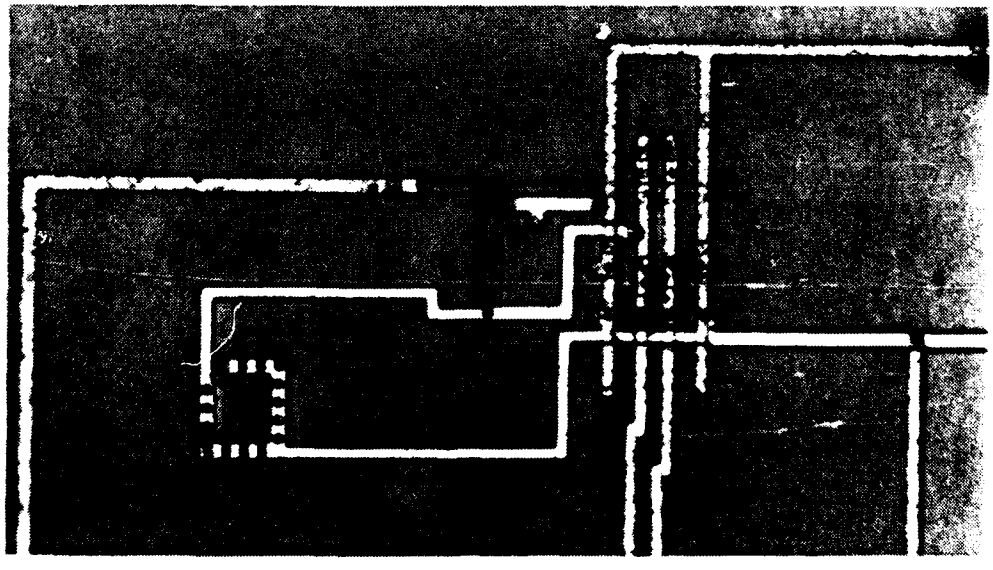


Figure 5-15. Photograph of a Detection and Storage Test Cell.

5.3.3 Experimental Results for Optically Written Logic Zero

The laser power required for optically writing a logic zero to the DATA node of a single detection and storage cell was determined experimentally. A Helium-Neon laser (λ = 0.6328 μm) was used as the light source in the experimental setup described in Appendix B. The output of the laser was focused into and out of a 15 μm diameter spatial filter by two 10X microscope objectives. A beam steering instrument composed of two mirrors directed the filtered beam to a 10X microscope objective and eyepiece, which then focused the light onto the chip containing the optoelectronic circuits. The final microscope objective and the chip were each mounted on an XYZ micropositioning stage.

The incident light was assumed to have the profile of a zero-order Gaussian beam, which had most of the noise removed by the 15 μm pinhole aperture of the spatial filter. Although the spot radius was estimated to be 30-45 μm, the results in this section are not adjusted for the relative areas of the light beam and the detector. This is because raw data is more easily supported by repeated experiments. Furthermore, methods of determining the beam spot size are not precise enough to support adjustment of data. The beam spot size is addressed in Appendix B.

The configuration in Fig. 5-16 illustrates the method for monitoring the optically written logic zero to the cell. To start the experiment, a variable beam splitter/attenuator was used to reduce the total power of the transmitted light to approximately 20 μW. With the word line connected to a 5 volt supply, the output of the BIT line buffer was monitored on an oscilloscope while the chip position was varied in the X-Y plane. Rough alignment of the beam and detector was achieved by positioning the chip to cause a change in the state of the BIT line output. The incident power was then reduced below the threshold required for changing the state of the cell. This allowed for a more precise alignment by adjusting the chip position until the maximum response to the optical input was obtained. Finally, the position of the chip was adjusted along the Z-axis to obtain the best response.

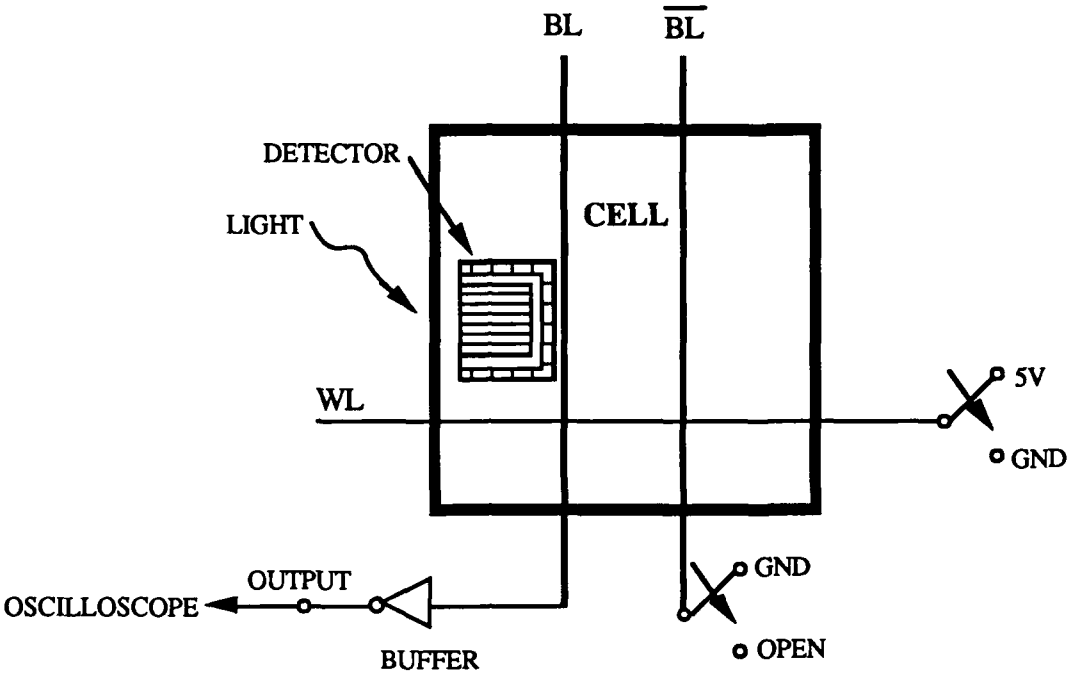


Figure 5-16. Experimental Circuit for Optically Written Logic Zero.

The first step in the general procedure for testing the detection and storage cell was to block the light source with an opaque object and set the DATA node to a logic one. This was accomplished by connecting the NOT BIT line to ground and then switching the word line to V_{DD}. Once the logic one was stored at the DATA node, the NOT BIT line was allowed to float. The opaque object was then removed from the beam path, exposing the detector to the optical signal. Two methods were used to take measurements of the DATA node voltage. During part of the experiment the BIT line voltage was continuously monitored on an oscilloscope while the word line was held high. When the word line was high, the BIT line was connected to the DATA node via the access transistor. A CMOS inverter on the same chip was used as an output buffer. This allowed observation of the transition of the DATA node voltage during the optical write operation, but added a small capacitance that had to be discharged along with the DATA node capacitance. Gradually

increasing the laser power caused the DATA node voltage to initially make a smooth transition to a slightly lower level and then pass through an unstable level before falling to a logic zero.

The optically written logic zero was also observed using a normal electrical read operation. The BIT lines and the word line were used to electrically set the DATA node to a logic one as previously described. With the word line low, the light source was then pulsed on and off. After the laser was turned off, the word line was raised to V_{DD} to transfer the stored information to the BIT line and output buffer. The laser power was increased after each read operation until a logic zero was transferred to the BIT line.

For both methods of measurement, the laser power required to optically write a logic zero was between 2.9 μW and 3.35 μW as shown in Fig. 5-17. The range of values is partially attributed to variations at the light source and in the alignment and focus of the

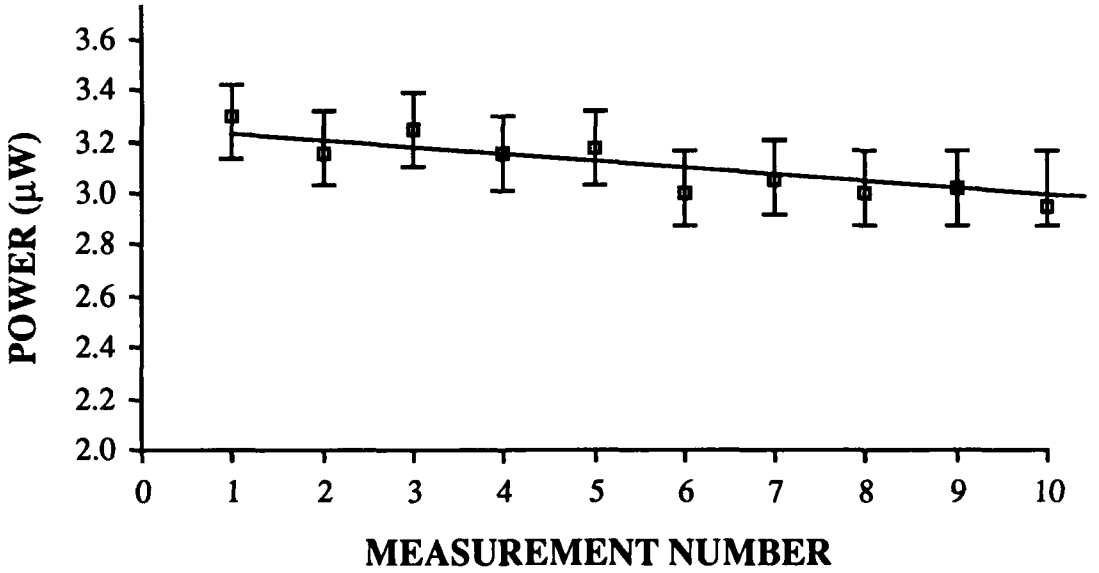


Figure 5-17. Light Beam Power Measurements for Optically Written Logic Zero. The data points are for an isolated optical detection and storage cell. Error bars are based on observed fluctuations in incident light power.

light beam. The method of measurement did not significantly affect the results. The low power measured for the single-cell optical write process agrees with the measured results for an array of cells discussed later in this chapter.

5.3.4 Detection and Storage of a Logic One

The difficulty in writing a logic one directly to the DATA node of a static RAM cell has already been mentioned. Circuits for writing a logic one are shown in Fig. 5-18. Figure 5-18(a) replaces the OWZ circuit with an optical circuit that passes a logic one directly to the DATA node. This circuit is likely to require a larger voltage on the gate of pass transistor T12 than its OWZ counterpart. A more practical method of writing a logic one to the DATA node is to write a logic zero to the NOT DATA using the circuits described in Section 5.2.1. In Fig 5-18(b), the OWZ circuit has been connected to the NOT DATA node instead of the DATA node. The operation of the circuit is similar to that of the detection and storage cell in Fig. 5-10.

Figure 5-19 is a combination of the circuits in Figs. 5-10 and 5-18(b). A single detector circuit writes a logic zero to either side of the cell. The appropriate node is selected by a control line which transfers the logic zero via a transmission gate or n-channel MOSFET. This circuit eliminates the need to electrically preset an array of cells to a logic one prior to transfer of data from a holographic ROM. A sequence of two optical write operations can set any bit pattern, regardless of the original states of the RAM cells. The first operation may be used to set the array to either all logic ones or all logic zeros. The next operation writes a zero or one to selected DATA nodes. This circuit reduces the amount of information that must be stored in the hologram. The complement of each DATA node bit pattern can be obtained by writing the same pattern to the NOT DATA nodes after all cells have been optically set to a logic zero. The control nodes may be electrically or optically switched on and off.

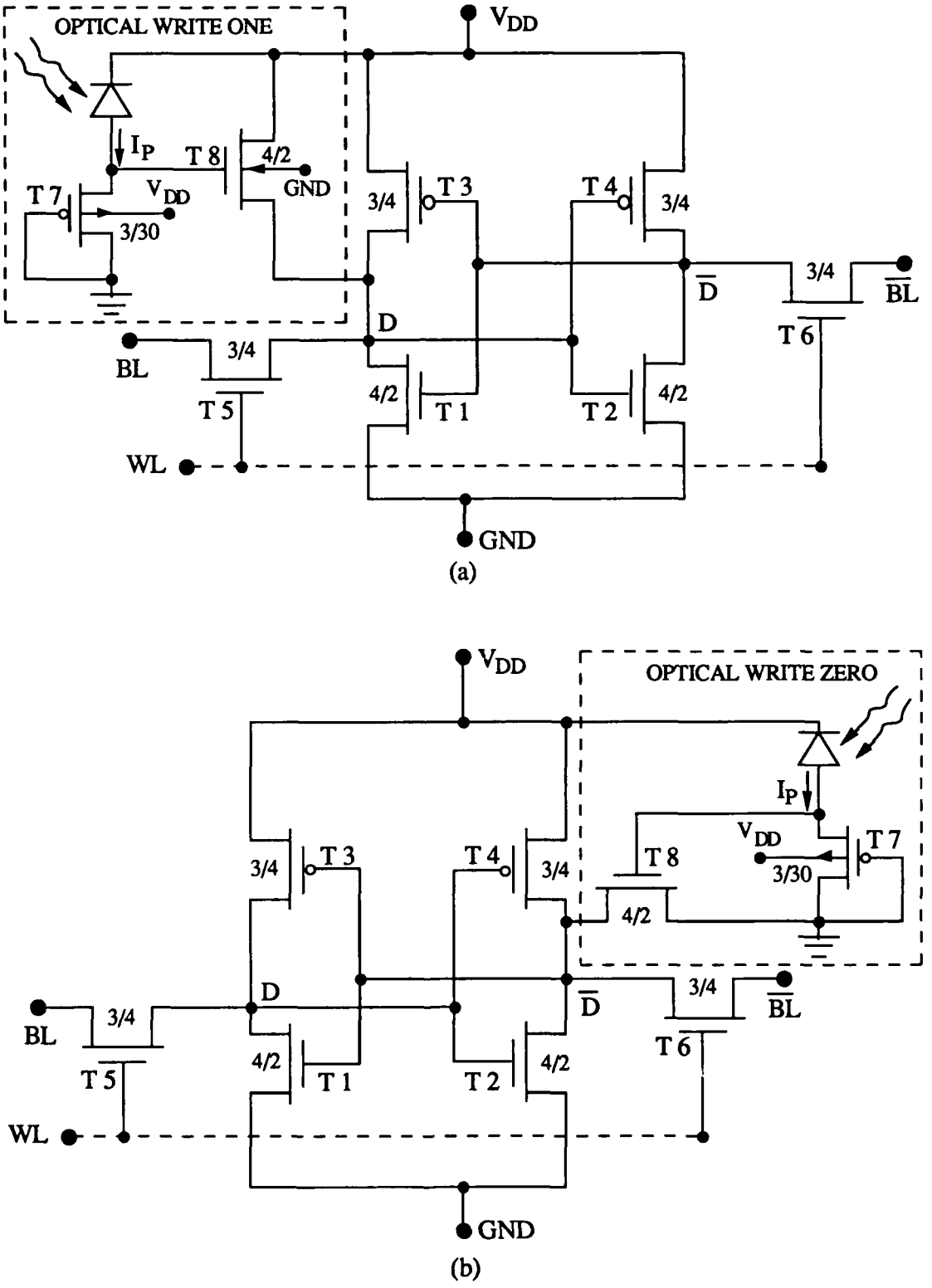


Figure 5-18. Circuits for Detecting and Storing an Optically Transmitted Logic One.

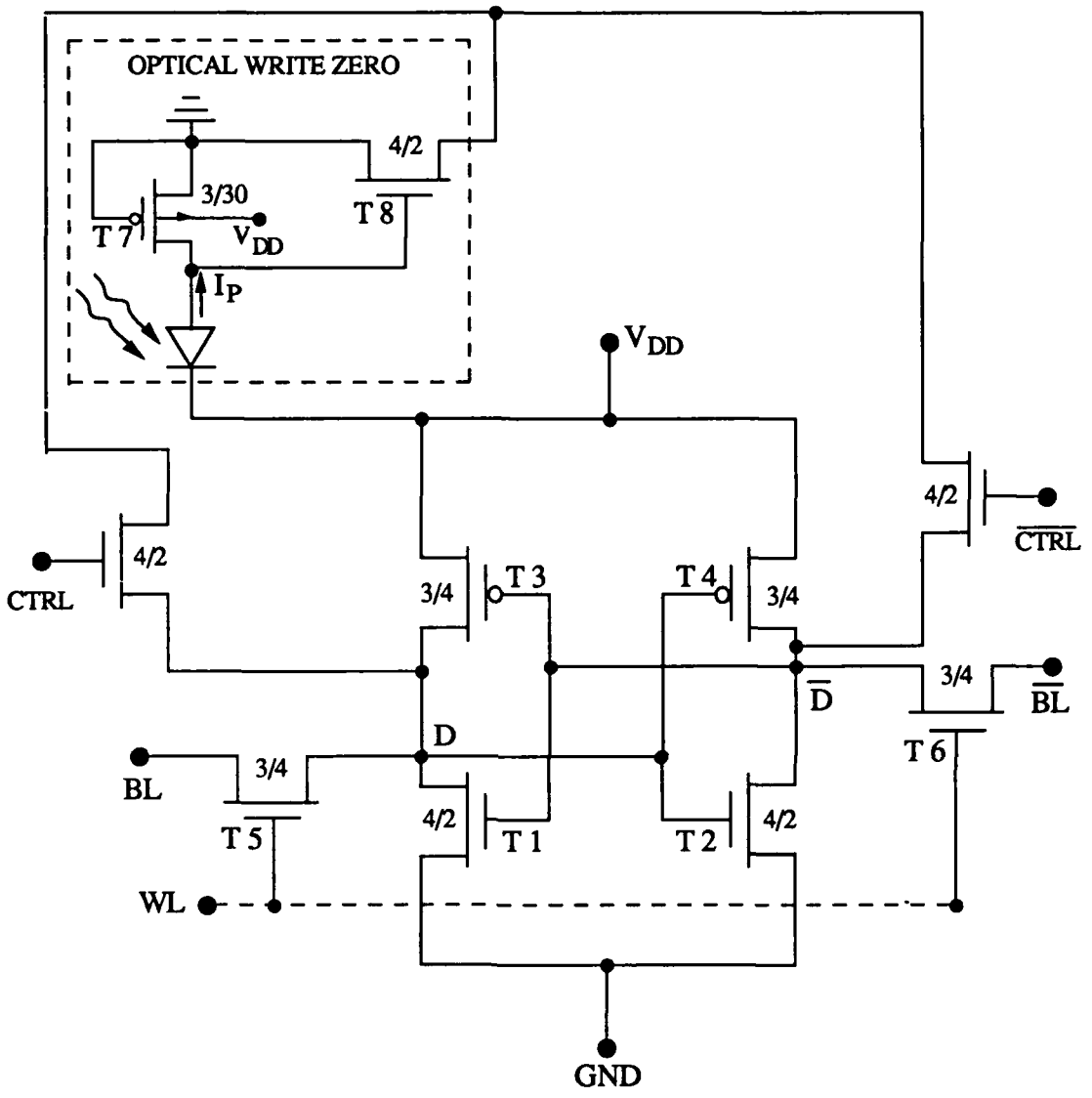


Figure 5-19. Cell for Storing Optical Information at DATA or NOT DATA Node.

5.4 Optical Detection and Storage Cell Array

A 4 x 4 array of the optical detection and storage cell in Fig. 5-10 was fabricated and tested. The 40-pin chip shown in Fig. 5-20 is 2200 μm wide and 2250 μm long. It contains the 400 μm x 400 μm storage cell array and a variety of other individual cells and detector circuits used for measurements. The substrate and p-wells are connected to V_{DD} and ground, respectively. The eight BIT and NOT BIT lines of the 4 x 4 array were

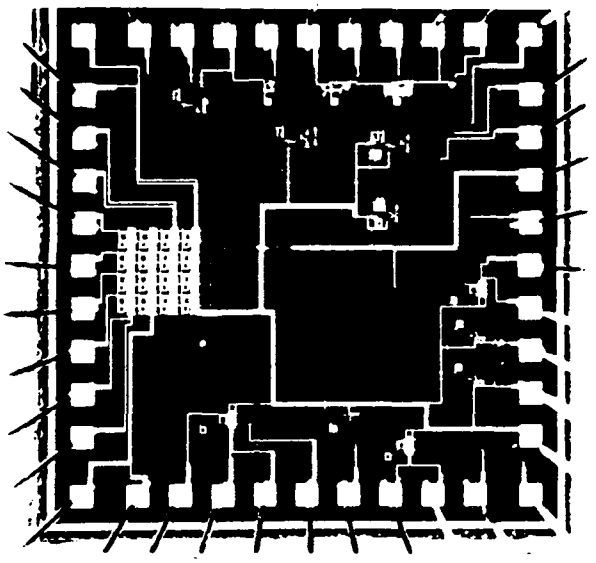


Figure 5-20. Photograph of Chip with Optical Detection and Storage Cell Array.

each connected to a bonding pad on the chip. Pins were also provided for individual access to the four word lines.

The detector array is organized as shown in Fig. 5-21. The 16 detectors in the array are drawn with scaled dimensions and spacing using the layout format of Fig. 5-14. All access and optical circuit transistors are shown in schematic form for simplicity. The cross-coupled inverters are shown as gate level symbols. Spacing is not to scale for the ground and BIT lines, which run vertically in the metal2 layer. The power supply bus runs horizontal except where it follows the shape of the guard ring.

Figure 5-22 is an isolated view of the storage cell array. A magnified view of a portion of the array is shown in Fig. 5-23. The PMOS load devices are visible just above the 16 detectors and guard rings. Some of the load transistors show a metal2 shield covering the channel. These metal rectangles were installed to reflect stray light away from the load device. No performance difference was observed between the devices with the shield and those without it. Measurements were taken via bonding pad connections.

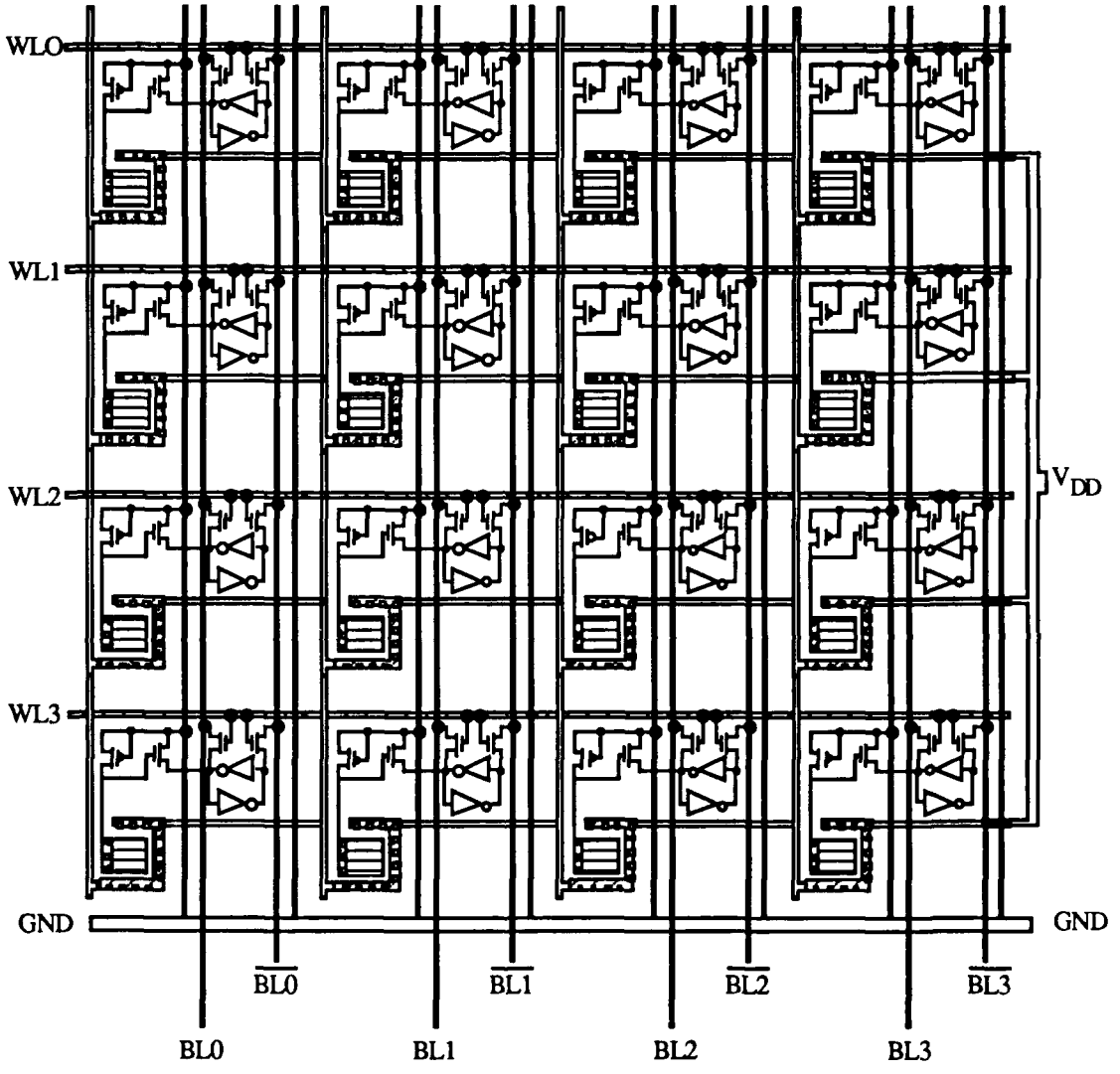


Figure 5-21. Schematic Diagram of 4 x 4 Cell Array.

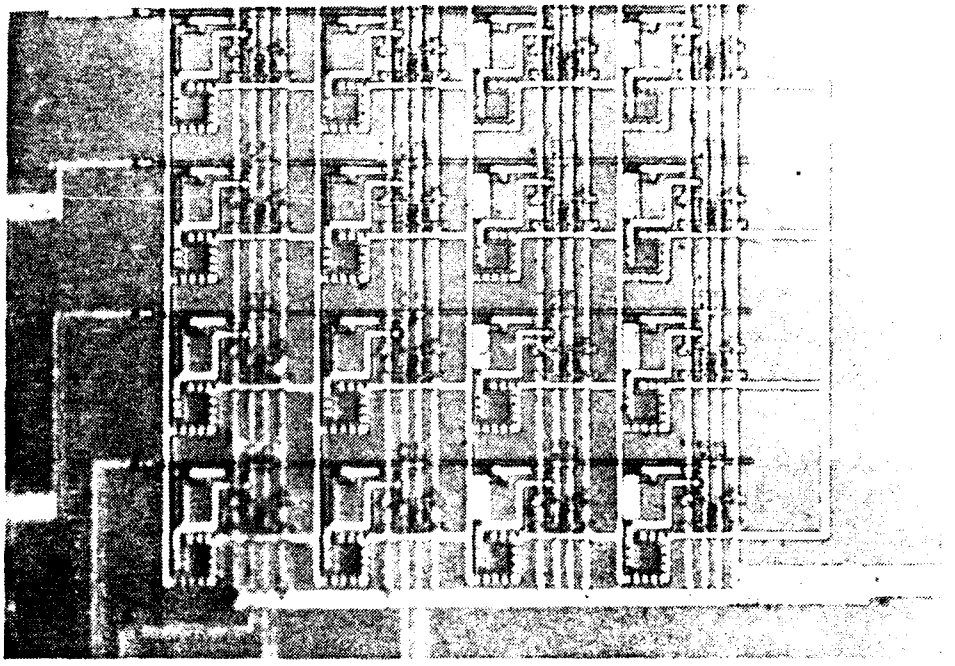


Figure 5-22. Photograph of 4 x 4 Optical Storage Cell Array.

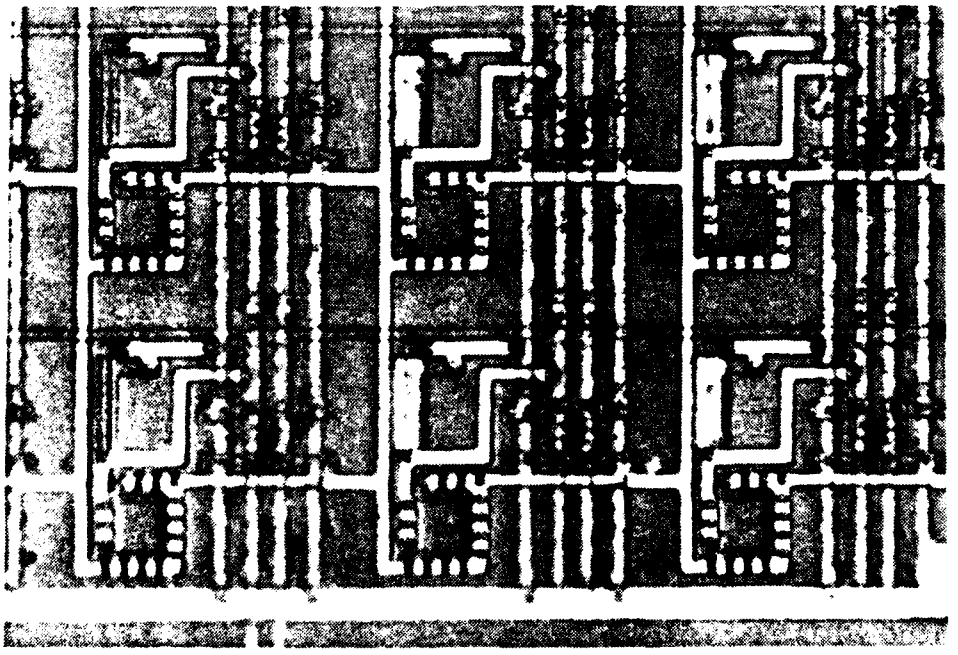


Figure 5-23. Enlarged Photograph of Optical Storage Cell Array.

The electrical and optical performance characteristics of the cells were determined experimentally. The electrical read and write operations of the array of cells were tested in the laboratory using a power supply, an oscilloscope, and a voltmeter. The stored data was measured via the access transistors and the BIT line. An integrated CMOS inverter was used as an output buffer. With the oscilloscope disconnected from the output, the NOT BIT line was connected to ground while the word line was connected to V_{DD}. The word line was then lowered to ground to allow connection of the oscilloscope to the BIT line. When the word line was again raised to 5 volts, the BIT line showed a logic one had been written to the DATA node. This complete procedure was repeated with the roles of the BIT line and the NOT BIT line reversed. Under these conditions, a logic zero was determined to have been written to the DATA node. The procedure for electrically writing a logic one was followed again to ensure a logic one could be written when the original state was a logic zero.

The optical write operation was tested using a 16-bit array of light beams. The beam pattern was established by an optical mask and focused on the cell array by a series of lenses. A 5 W Argon laser was used for this experiment because it is the primary light source used in the development of the holograms for optical ROM-to-electronic RAM data transfer research. Generally, the quantum efficiency of silicon detectors is lower at the Argon emission wavelength of 0.5145 μm than at longer wavelengths up to 0.8 μm [53]. This is attributed to the increased absorption near the surface for shorter wavelengths. Carriers generated near the surface are more likely to recombine instead of contributing to the photocurrent. From equation (3.4), the number of photon-generated carriers absorbed is proportional to $(1-e^{-\alpha x})$, where α is the absorption coefficient and x is the distance into the silicon device. Using Fig. 3-8, the approximate values of α for Helium-Neon and Argon are 0.5 and 0.9 $[\mu m]^{-1}$, respectively. Based on these values, the percent of photons absorbed is shown in Fig. 5-24 for distances corresponding to the approximate junction

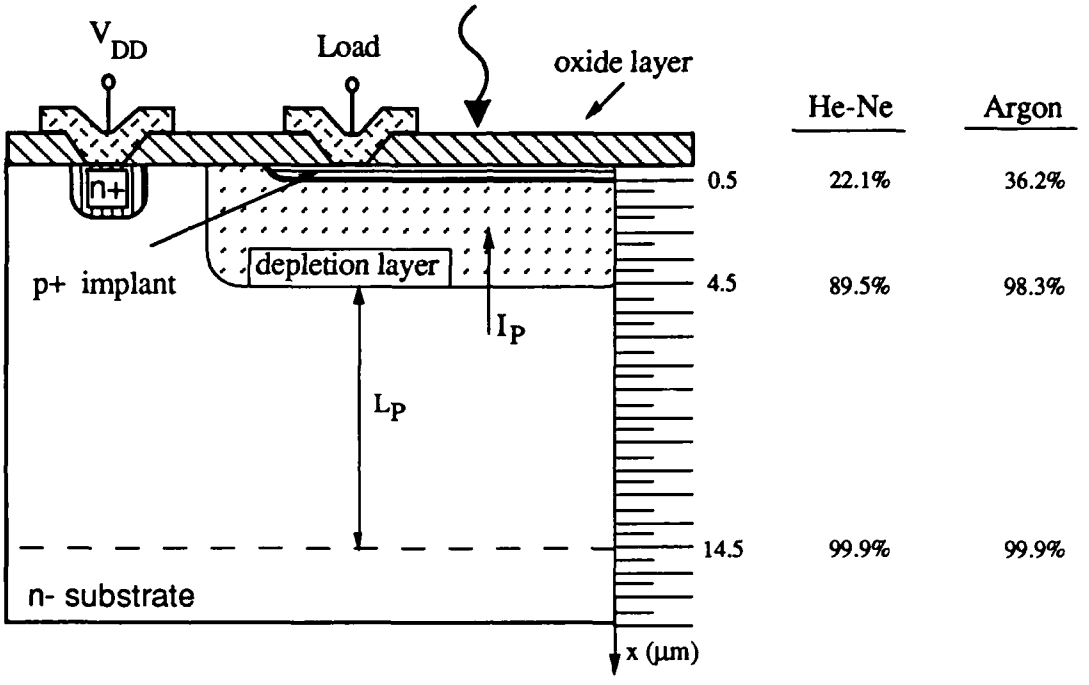


Figure 5-24. Photon Absorption Profile for He-Ne and Argon Lasers. The plot assumes a p^+n^- photodiode with a reverse bias voltage of 5 V.

and depletion layer depths, and one hole diffusion length into the substrate. Inspection of the absorption profile in the figure reveals the response of the detector to the Argon laser should be similar to the response to the He-Ne laser. The number of photons absorbed in the depletion layer is 62% and 67%, respectively. When diffusion from the substrate is considered, the He-Ne laser generates slightly more carriers that contribute to the photocurrent than the Argon laser.

Optically written logic zeros were observed for each of the three patterns in Fig. 5-25. The measurements were taken according to the chart in Fig. 5-26. The Argon laser output was directed onto the cell array via a series of beam steering mirrors, a beam splitter/attenuator, and a 50 μm spatial filter pinhole. The light beam was focused with two optical glass lenses. The chip was mounted on a circuit board, which was clipped to a 360 degree rotation stage. The rotation stage was mounted on an XYZ micropositioning stage.

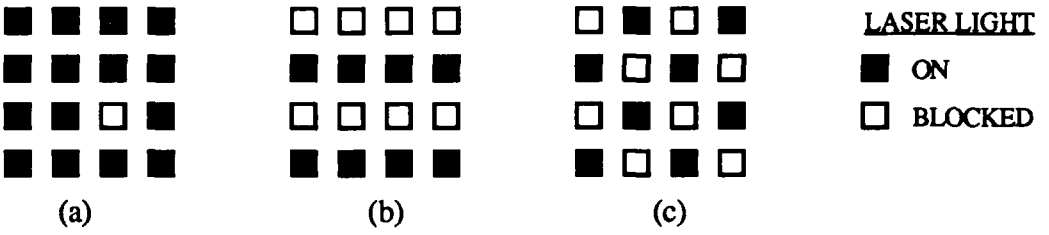


Figure 5-25. Light Patterns Used to Test Optical Detection and Storage Cell Array.

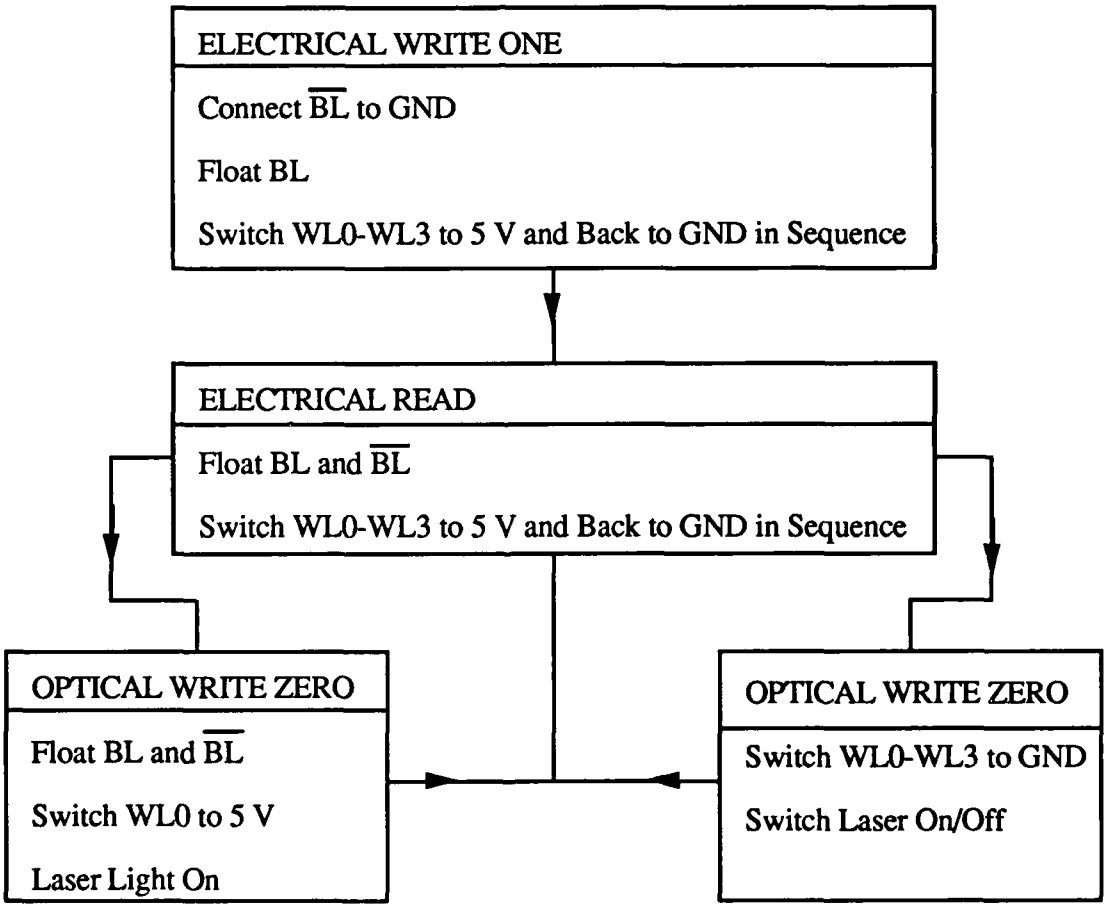


Figure 5-26. Flowchart for Testing Optical Detection and Storage Cell Array.

As shown in Fig. 5-26, the transfer of optical data was verified using the electrical read operation. In this procedure, all cells were electrically set to a logic one. With the word lines held low, the light source was turned on and off. After the laser was turned off, the DATA nodes were read electrically by individually pulsing the word lines to a logic one. The optical write process was also observed while continuously monitoring selected DATA nodes.

The output of the memory cell array to the BIT lines was observed using an external circuit specifically designed for that purpose. The output circuit was made up of commercially available CMOS and TTL integrated circuits and light emitting diodes (LED). An LED display was arranged in a 4 x 4 array similar to the memory array. When the LED for a particular bit was on, the corresponding DATA node was storing a logic one. The light turned off when the logic zero was written. The output circuit allowed monitoring of one complete row of the cell array at a time without significantly loading the BIT lines. The output display circuit is described in Appendix D.

All electrical and optical operations tested during the experiments worked as designed. The laser power required for the pattern in Fig. 5-25(a) was 50.2 μW. This gives an average of 3.35 μW for each of the 15 illuminated pixels. No adjacent cell interference was recorded for any of the patterns tested. These results are consistent with the experimental data provided in Section 5.3.3 for a single cell. The laser power levels were similar, although a He-Ne laser was used for those experiments.

5.5 Optical Detection and Storage Cell Analysis

Although the optical and electrical operation of the detection and storage cell in Section 5.3.1 has been discussed, very little attention has been given to the effects of the optical circuit on the electrical SRAM cell operations. The obvious effects include the addition of an NMOS device drain capacitance to the DATA node. The overlap capacitance

and drain-bulk capacitance calculate to be approximately 6.55 fF when a logic one is stored at the DATA node and 13.5 fF for a logic zero. The cell capacitance is discussed in detail in Section 5.5.2.

Another effect is that the logic one voltage at the DATA node may be slightly less than V_{DD} because of current leakage. As discussed in Chapter 4, the dark output voltage (~1.3 V) of the detector and saturated PMOS load circuit is slightly greater than the n-channel transistor threshold voltage. This causes transistor T8 in Fig. 5-9 to be barely on under dark conditions. Although the DATA node voltage could not be measured directly in the laboratory, simulation results give a value of 4.77 volts. For the applications in this thesis, this effect is ignored.

Under some conditions, other interaction may occur between the optical and the electrical components of the storage cell. This section considers the effects of the optical circuit on the electrical operation of the cell when both circuits are active. Although not the main focus of this work, the transient response of the optical circuit will also be addressed.

5.5.1 Optical Circuit Effects on Cell Operation

The SRAM cell with optical write capability was independently tested for proper electrical and optical operation. Due to the possibility of the optical circuit being activated by BIT or word line coupling, electromagnetic interference, or optical noise, the effects of this phenomena on electrical read and write operations have been investigated. In the following paragraphs, the photocircuit portion of Fig. 5-10 is assumed to be temporarily, but unintentionally, active during the electrical operation of the SRAM cell.

5.5.1.1 Electrical WRITE ZERO

The circuit in Fig. 5-27 gives the disposition of the data storage cell at the start of WRITE ZERO. The existing state is assumed to be a logic one. If the photocircuit access transistor temporarily turns on during the write cycle, T8 simply shunts T5 and T1 and

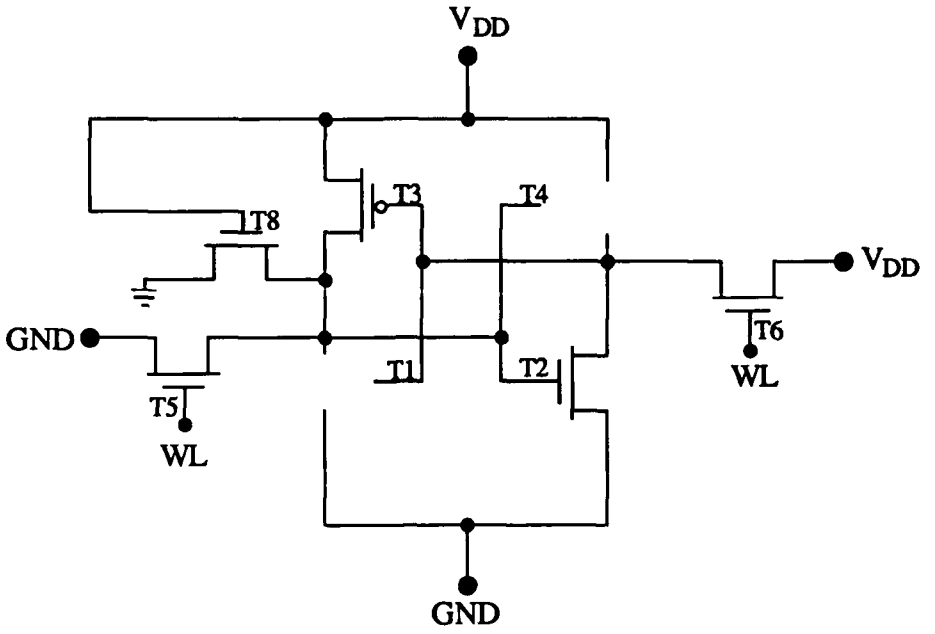


Figure 5-27. Detection and Storage Cell at the Start of Electrical WRITE ZERO.

speeds up the writing of the logic zero. At the end of the write operation, T3 is in cutoff. The current flow through the DATA node is approximated by $I_{Sp} = I_{Dn} = 0$, where I_{Dn} is the total current in T1, T5, an T8. This gives $V_{DATA} \approx 0$, which is the normal output low voltage for a CMOS inverter. For this operation, the photocircuit has minimal impact on the electrical operation of the cell.

5.5.1.2 Electrical READ ZERO

The initial state of the storage cell during READ ZERO is shown in Fig. 5-28. Although the BIT line at T5 will actually discharge during the read access, it is assumed to remain at the supply voltage level to obtain worst case conditions for this analysis. If the photocircuit is coupled to the BIT line or word line, T8 may temporarily turn on at the start of the read cycle. Again, the gate of T8 is simply connected to the supply voltage to approximate the worst case. As shown in Fig. 5-28, T8 shunts T1 and reduces the effective resistance of the driver circuit. This is equivalent to increasing the aspect ratio of

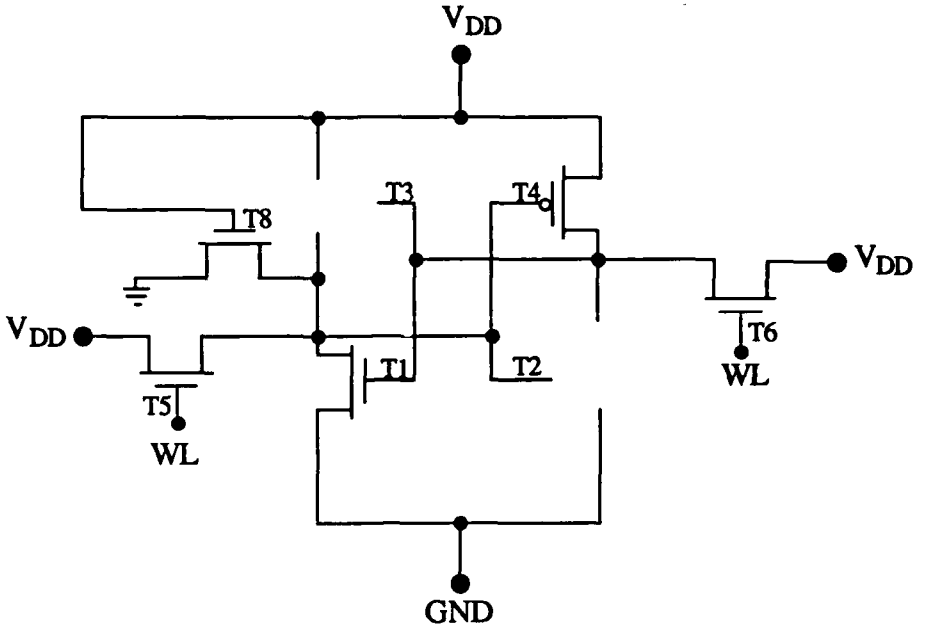


Figure 5-28. Detection and Storage Cell at the Start of READ ZERO.

T1, which reduces the output low voltage of the enhancement load inverter formed by T5 and T1. This can be shown by summing the current at the DATA node, which gives

$$I_{D5} = I_{D1} + I_{D8} \tag{5.7}$$

where $I_{Sp} = 0$ is assumed and the numerical subscripts correspond to the devices in the circuit. Transistor T5 is saturated, while T1 and T8 are nonsaturated. Substituting the respective drain current equations gives

$$\left(\frac{W}{L}\right)_{T5}\left[V_{DD} - V_X - V_{Tn}(V_X)\right]^2 = \left(\frac{W}{L}\right)_{T1}\left[2(V_{DD} - V_{Tn})V_X - V_X^2\right] + \left(\frac{W}{L}\right)_{T8}\left[2(V_{DD} - V_{Tn})V_X - V_X^2\right], \tag{5.8}$$

where V_X is the voltage at the DATA node and body-bias effects are included. Using aspect ratios from Fig. 5-10 and numerical parameters from Table A-1, an iterative solution for $V_{DD} = 5$ V gives $V_X = 0.302$ volts. This value, which is consistent with expectations, can be compared with $V_{OL} = 0.51$ volts without the optical circuit as given in Table 2-3. Thus, the optical circuit does not have a negative effect on this electrical operation of the cell.

5.5.1.3 Electrical WRITE ONE

The electrical WRITE ONE cycle is assumed to start with the storage cell at a logic zero state as in Fig. 5-28. The bit line at T6 is discharged to a logic zero, while T5 remains connected to a logic one. The disposition of the cell at the start of WRITE ONE is shown in Fig. 5-29. Initially, T8 shunts T1 as during READ ZERO; however, for the write operation, T1 must eventually be turned off by the logic zero applied at T6. Thus, the access transistor T5 and the photocircuit transistor T8 form an inverter with a saturated

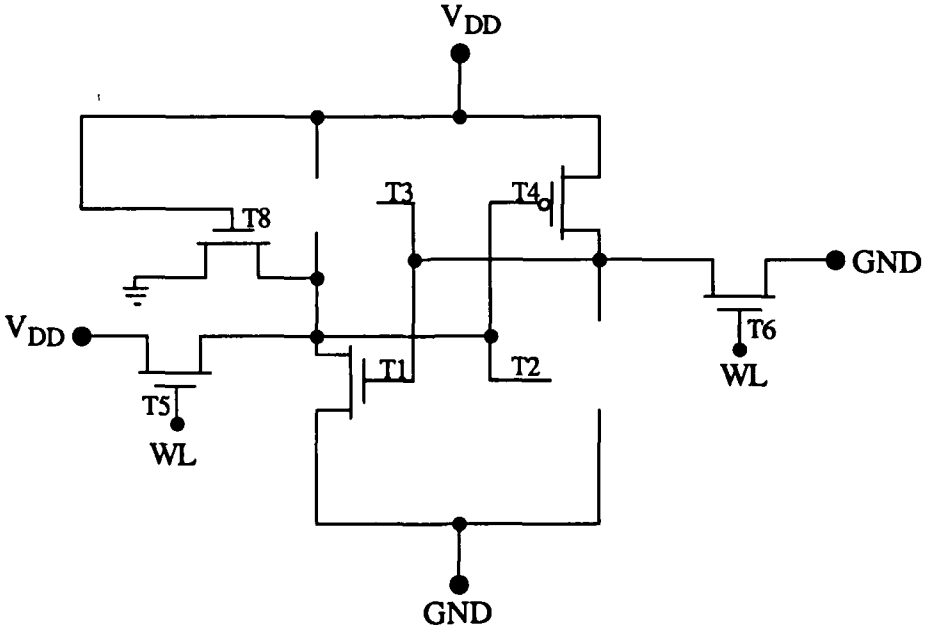


Figure 5-29. Detection and Storage Cell at the Start of WRITE ONE.

enhancement mode load. Transistor T5 is in parallel with T3, which turns on when the logic one is written. For the logic one to be written under worst case conditions the T3/T5/T8 inverter should have an output low voltage V_{OLW} as large as possible. Since the two CMOS inverters are cross-coupled and a logic zero is being written to the opposite data node, V_{OLW} for the T3/T5/T8 inverter must be at least greater than the input low voltage for the CMOS inverters. Summing currents at the DATA node and assuming T3 is nonsaturated ($V_{DATA} = V_X \geq |V_{Tp}|$), the analysis equation becomes

$$\left(\frac{W}{L}\right)_{T5}\left[V_{DD} - V_X - V_{Tn}(V_X)\right]^2 = \left(\frac{W}{L}\right)_{T8}\left[2(V_{DD} - V_{Tn})V_X - V_X^2\right]$$

$$- \frac{k'_p}{k'_n}\left(\frac{W}{L}\right)_{T3}\left[2(V_{DD} + V_{Tp})(V_{DD} - V_X) - (V_{DD} - V_X)^2\right] \qquad (5.9)$$

where body-bias effects are considered. When $V_{DD} = 5$ V, an iterative solution is gives $V_X = 0.78$ V. For the electrical WRITE ONE to overcome the effects of the optical circuit, this value of $V_X = V_{OLW}$ needed to be greater than $V_{IL} = 1.37$ volts as provided in Table 2-3.

The output low voltage analysis in Chapter 2 for the access inverter with T1 as the driver also applies to the access inverter with T8 as the driver when the current of T3 is neglected. The output low voltage increases when the size of T8 decreases. Referring to Table 2-3 and Fig. 2-6, the value for $(W/L)_{T8}$ needs to be less than 3/4 when all other devices remain unchanged. Since V_{OLW} will be greater than V_{IL} for the CMOS inverter, a logic one may be written electrically despite the temporary state of the optical circuit. The optical noise margin (NMO) for WRITE ONE will be defined as $NMO = V_{OLW} - V_{IL}$.

The tradeoffs necessary to satisfy the requirements in this section are significant. Although the analysis assumes the gate voltage of T8 is at the supply rail, this is not likely

to occur. The analysis may be repeated with a lower gate voltage. In this case, the channel resistance of T8 increases and V_{OLW} becomes larger, which permits a larger $(W/L)_{T8}$. Making the channel of T8 longer, reduces the ability of the optical circuit to sink current from T3 and discharge the capacitance of the DATA node in a timely manner.

5.5.1.4 Electrical READ ONE

The configuration of the storage cell at the start of READ ONE is shown in Fig. 5-30. The access transistor T5 shunts T3 when the word line is turned on. If the photocircuit is coupled to the word line or the BIT line, T8 may temporarily turn on during the read access. When T8 is on, it acts as the driver for an inverter which has T5 and T3 as load devices. The output low voltage of the T5/T3/T8 inverter must remain above the threshold voltage of the CMOS inverter. For READ ONE, the minimum voltage is the CMOS inverter threshold V_{th} instead of V_{IL} because a logic zero is not being simultaneously written to the opposite data node as occurs in WRITE ONE. This

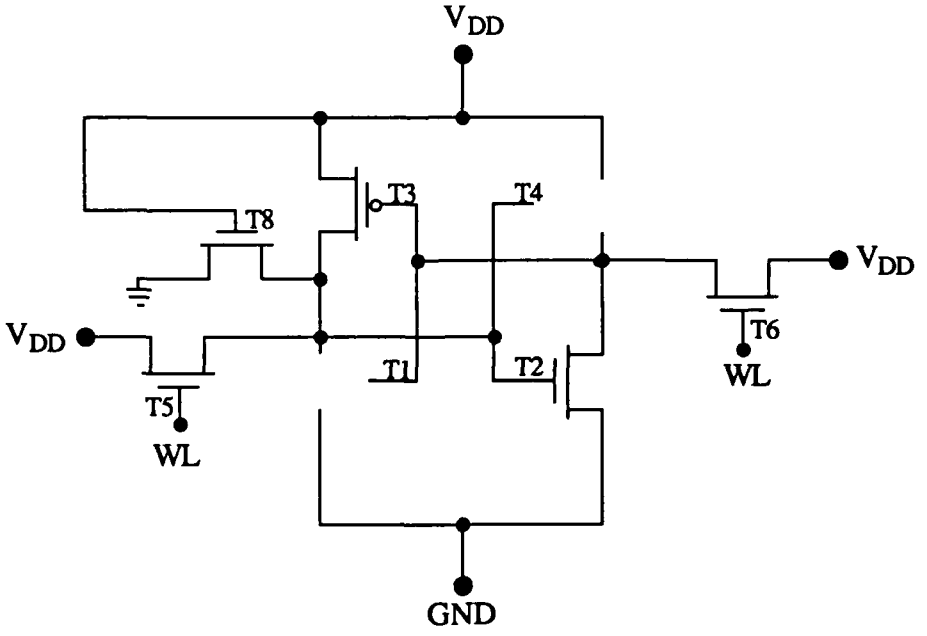


Figure 5-30. Detection and Storage Cell at the Start of READ ONE.

restriction will significantly reduce the aspect ratio of T8. The impact may be reduced by including T3 as a load device instead of neglecting it as in the last section. Retaining T3 increases the design value of the T5/T3/T8 inverter low output voltage V_{OLR}, which allows a larger aspect ratio for T8.

The value of V_{OLR} may be determined by summing the currents at the DATA node. With T8 and T3 in the nonsaturated mode and T5 saturated, the KCL equation is

$$\left[2(V_{DD} - V_{Tn})V_{OLR} - V_{OLR}^2\right] = \frac{\beta_{T5}}{\beta_{T8}}\left[(V_{DD} - V_{OLR}) - V_{Tn}(V_{OLR})\right]^2 + \frac{\beta_p}{\beta_{T8}}\left[2(V_{DD} + V_{Tp})(V_{DD} - V_{OLR}) - (V_{DD} - V_{OLR})^2\right] \quad (5.10)$$

where V_{OLR} is the output low voltage to be determined. With body bias effects included for T5, equation (5.10) must be solved by iteration in conjunction with the access transistor threshold voltage given by

$$V_{Tn}(V_{OLR}) = V_{TO\,n} + \gamma\left(\sqrt{V_{OLR} + 2|\phi_F|} - \sqrt{2|\phi_F|}\right) \quad (5.11)$$

where $V_{Tn}(V_{OLR})$ implies V_{Tn} is a function of V_{OLR}. The solution to equation (5.10) is $V_{OLR} = 0.78$ V. Repetitive solutions for smaller aspect ratios for T8 will show that the aspect ratio of T8 must be reduced below 3/4 to satisfy $V_{OLR} > V_{th}$. Since this was not a worst case calculation, V_{OLR} should also include a small margin for error.

The aspect ratio for T8 based on V_{OLR} is smaller than the maximum value based on V_{OLW}. A successful electrical READ ONE with the optical circuit active implies a successful WRITE ONE and all other electrical operations under the same conditions. The

conditions described in this section are not required for the design of all optical detection and storage cells. The cell design procedure depends on the application. The detection and storage cells presented in this chapter and used for experimentation are not designed based on this analysis.

5.5.2 Optical Circuit Transient Response

The transient response of the detection and storage cell in Fig. 5-10 to an input photocurrent is the total response time for a memory array since information is transmitted in parallel. The speed at which optically transmitted data is written does not depend on the number of storage cells accessed. Thus, the time saved when data is written in parallel instead of sequentially increases with the size of the memory. Verification of the optical access time for a single cell will allow comparison of the optical write time with the electrical write time for any size memory array.

The response of the storage cell to a photonic input is complex since more than one capacitive node is charging or discharging during the optical write process. In Fig. 5-10, the NOT DATA node voltage rises while the DATA node voltage falls. The NOT DATA node controls the gates of T1 and T3 during the write operation. Changes in the gate voltage as well as the drain-source voltage cause variations in the channel conductance of these devices. This affects the flow of current from the DATA node and the rate at which the node capacitance discharges.

The time needed to write a logic zero also depends on the response of the optical circuit. When light is incident on the detector, the gate voltage of T8 rises at a rate determined by the source node of T7. As the gate voltage increases, the drain voltage of T8 decreases, along with the DATA node voltage. At a given time point, the source-drain voltage of T7 depends on the capacitance at the source node, the resistance of the channel, and the magnitude of the photocurrent. The voltage at this node is further complicated by

the changing photocurrent magnitude as carriers diffuse from the substrate to the depletion layer of the detector.

In the next paragraphs, several expressions that represent the starting point for seeking an approximate solution to the transient behavior of the cell during the optical write process are given. For circumstances in which an analytical solution is preferred over a SPICE simulation, some of the expressions may be simplified by assumptions. The components of the total capacitance at the DATA node are provided later in this section. For simplification, the capacitance is initially assumed to be a single fixed value. Summing currents at the DATA node then gives

$$I_{D8} = (I_{S3} - I_{D1}) - C_{DATA} \frac{dV_{data}}{dt}, \tag{5.12}$$

where all transistor currents are a function of time-dependent V_{data} as well as a time-dependent gate voltage. The drain current of access transistor T5 is neglected since the device is in cutoff. The drain current of T1 is small, but not necessarily small enough to be neglected. At the start of the optical write operation, I_{D1} is negligible because T1 is in cutoff. At the end of the write cycle, the current in T1 is again small because T3 is in cutoff. However, at some point during the transition both devices are on, which causes a significant current flow in T1. This current speeds up the discharge time for C_{DATA} since T1 is in parallel with T8. Thus, neglecting I_{D1} would give a conservative estimate of the response time.

During the optically written logic zero, the initial drain current of T8 is given by [51]

$$I_{D8} = \frac{\beta_n}{2}(V_{GS8} - V_{TO_n})^2 \tag{5.13}$$

where channel-length modulation is neglected. When the DATA node voltage drops such that $V_{DATA} \leq V_{GS8} - V_{TOn}$, the nonsaturation drain current becomes

$$I_{D8} = \frac{\beta_n}{2}\left[2(V_{GS8} - V_{Tn})V_{DATA} - (V_{DATA})^2\right]. \tag{5.14}$$

Equation (5.14) only applies for a short duration since $V_{GS8} \approx 2$ V and $V_{Tp} = 1$ V. If the optical write process ends when the DATA node reaches V_{IL} for the cross-coupled inverters, then nonsaturation may not occur if $V_{IL} \geq 1$ V. Transistor T3 is in the nonsaturation region of operation at the start of the optical write process. The current as a function of the DATA and NOT DATA node voltages is determined by

$$I_{S3} = \frac{\beta_p}{2}\left[2(V_{DD} - V_{\overline{DATA}} + V_{Tp})(V_{DD} - V_{DATA}) - (V_{DD} - V_{DATA})^2\right] \tag{5.15}$$

where $V_{\overline{DATA}}$ is the voltage at the NOT DATA node. During the transition of the DATA node voltage, T3 becomes saturated such that

$$I_{S3} = \frac{\beta_p}{2}(V_{DD} - V_{\overline{DATA}} + V_{Tp})^2. \tag{5.16}$$

The set of analysis equations can be completed by adding the equation for the drain current of T1 for the saturation and nonsaturation regions of operation and the expression for V_{GS8} as a function of the photocurrent given in equation (5.5). An optimistic estimate of the discharge time of the DATA node can be found by assuming the drain current of T1 is equal the source current of T3. Equation (5.12) is then reduced to

$$I_{D8} = - C_{DATA} \frac{dV_{data}}{dt} . \tag{5.17}$$

Substituting equation (5.8) and assuming a linear average value for V_{GS8} gives

$$\frac{\beta_n}{2}(V_{GS8} - V_{Tn})^2 = - C_{DATA} \frac{dV_{data}}{dt} . \tag{5.18}$$

Transistor T8 is in saturation until $V_{DATA} = V_{GS8} - V_{Tn}$. Making that substitution and integrating gives

$$t_{SAT} = - C_{DATA} \int_{V_{DD}}^{V_{GS8} - V_{Tn}} \frac{2\, dV_{data}}{\beta_n (V_{GS8} - V_{Tn})^2} , \tag{5.19}$$

where t_{SAT} is the discharge time while T8 is in saturation. Evaluating the integral gives

$$t_{SAT} = C_{DATA} \frac{2(V_{DD} + V_{Tn} - V_{GS8})}{\beta_n (V_{GS8} - V_{Tn})^2} . \tag{5.20}$$

Using equation (5.14) with V_{DATA} replaced by V_{data}, an expression can also be found for the discharge time when T8 is in the nonsaturation region of operation. The results give [51]

$$t_{NONSAT} = \frac{C_{DATA}}{\beta_n (V_{GS8} - V_{Tn})} \ln\left[\frac{2(V_{GS8} - V_{Tn})}{V_{IL}} - 1\right], \tag{5.21}$$

where the logic zero is written when V_{DATA} reaches the input low voltage V_{IL} of the cross-coupled inverters. Equations (5.20) and (5.21) may be combined to give the total estimated time for transition of the DATA node from a logic one to a logic zero during the optical write process.

The capacitance of the circuit affected by the optically written logic zero is shown in Fig. 5-31. The response time of the circuit to a low power optical input can be estimated by treating the rise time of the gate of T8 and the fall time of the DATA node as two separate events. The rise time of the gate of T8 will be considered first. An expression for the transient time interval will be determined and then evaluated using experimental data and the SPICE model parameters provided in Table A-1.

The photocurrent provides the source current of transistor T7 and charges the

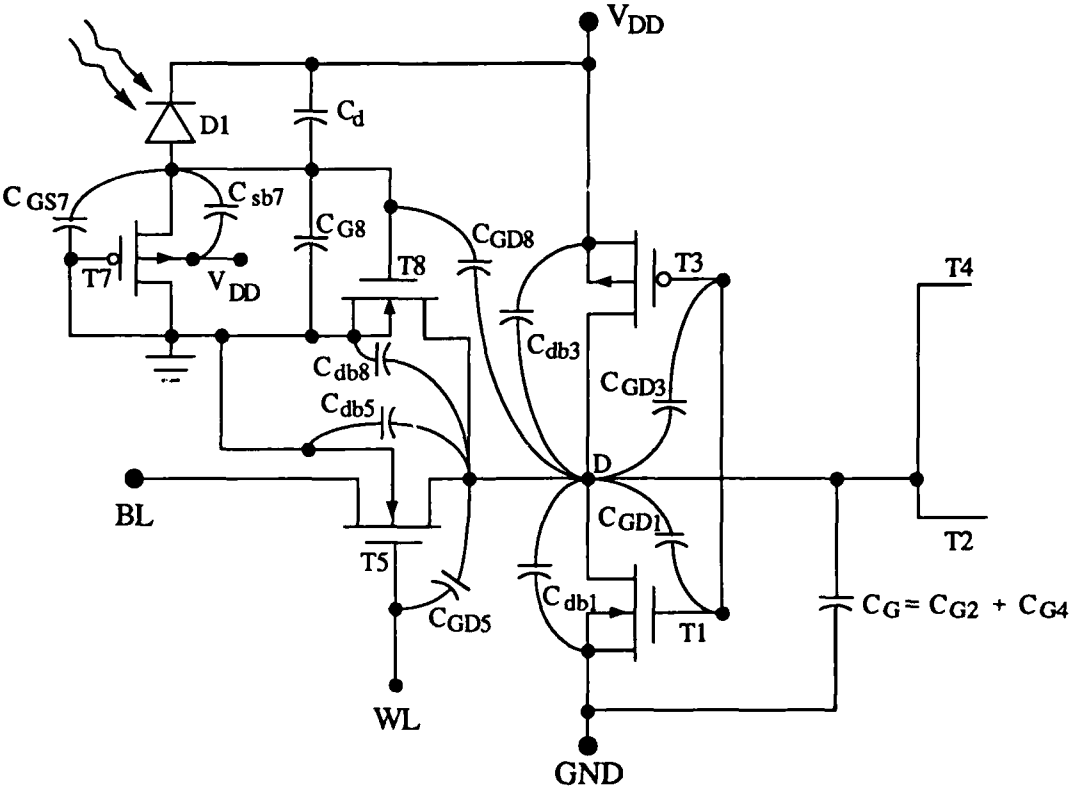


Figure 5-31. Capacitance Associated with the Optically Written Logic Zero.

capacitance at the gate of T8. The currents at the source node of T7 are summed to obtain

$$I_{S7} - I_P = C_d \frac{d(V_{DD} - V_L)}{dt} + C_{sb7} \frac{d(V_{DD} - V_L)}{dt} - C_{GS7} \frac{dV_L}{dt} - C_{G8} \frac{dV_L}{dt} \qquad (5.22)$$

where I_{S7} is the source current of T7 and V_L is the gate voltage of T8. Equation (5.22) can be written as

$$I_{S7} - I_P = -(C_d + C_{sb7} + C_{GS7} + C_{G8}) \frac{dV_L}{dt} \qquad (5.23)$$

or

$$t = -(C_d + C_{sb7} + C_{GS7} + C_{G8}) \int_{1.3}^{2.0} \frac{dV_L}{\frac{\beta_p}{2}(V_L + V_{Tp})^2 - I_P} \qquad (5.24)$$

where the expression for saturated drain current has been substituted for I_{S7} and body-bias is temporarily neglected. Evaluating the integral gives

$$t = \frac{2}{\beta_p}(C_d + C_{sb7} + C_{GS7} + C_{G8}) \left[\frac{1}{2\sqrt{\frac{2I_P}{\beta_p}}} \ln \left(\frac{\sqrt{\frac{2I_P}{\beta_p}} + (V_L + V_{Tp})}{\sqrt{\frac{2I_P}{\beta_p}} - (V_L + V_{Tp})} \right) \right]_{1.3}^{2.0} \qquad (5.25)$$

where the integration limits are based on experimental results provided in Fig. 4-16. The capacitance values are determined from the model parameters in Table A-1 and the dimensions provided in Table 5-1. When the capacitance is voltage-dependent, the largest possible value is used.

The total capacitance in equation (5.25) is 105.16 fF. Approximately 40% of the total capacitance is due to C_d. The photocurrent is determined from the product of experimental values of responsivity and laser power. Responsivity is given as 0.178 A/W in Chapter 3. The incident laser power of 3.35 μW is in Section 5.3. Evaluating the equation for $(W/L)_p = 3/30$ and $I_P = 0.596$ μA, the theoretical time interval is 206.4 ns. Although this response time is large, several factors should be considered. The method of calculation included worst case values for the capacitance. Also the photocurrent was not based on a direct measurement from the storage cell and is most likely a conservative value.

Table 5-1. Dimensions of Devices in the Optical Detection and Storage Cell

DEVICE	AD $(\mu m)^2$	PD (μm)	AS $(\mu m)^2$	PS (μm)	W (μm)	L (μm)
T1	92.00	64.5	185.0	74.5	4	2
T2	92.00	64.5	21.00	18.5	4	2
T3	22.75	19.5	22.75	19.5	3	4
T4	22.75	19.5	22.75	19.5	3	4
T5	39.75	31.5	22.75	19.5	3	4
T6	39.75	31.5	22.75	19.5	3	4
T7	43.75	34.5	19.75	18.5	3	30
T8	13.00	14.5	101.0	58.5	4	2
D1	320.0	72.0			16	20

The response time can be improved by a smaller detector, a smaller gate area for T7, or a larger photocurrent.

The second phase of the optically written logic zero occurs when the gate of T8 has reached 2 volts. At this point the DATA node discharges through T8 to approximately zero volts. The response time is estimated from equations (5.20) and (5.21) after the capacitance at the DATA node is known. The linear average capacitance values are given in Table 5-2, as determined from the device dimensions in Table 5-1 and the parameters in Table A-1. Neglecting line capacitance, the total average node capacitance is 94.94 fF. This gives an approximate DATA node discharge time of 8.76 ns, where t_{SAT} = 6.88 ns and t_{NONSAT} = 1.88 ns. The maximum time for the optically written logic zero is then 215 ns. The focus of improvements to the cell should be on the detector and load circuit since most of the delay occurs in that part of the cell. The response time of the detector is inversely proportional to the photocurrent. Thus, the response time decreases when the laser power is increased during the optical write process. The cell can be improved with a smaller detector and a correspondingly smaller beam spot size, while the incident power remains constant. If the channel length of T7 is reduced, the magnitude of the photocurrent must increase to obtain the same maximum source-drain voltage. The load device can be optimized by reducing the channel length until the maximum detector output voltage for a given photocurrent is equal to the minimum required gate voltage for T8.

Table 5-2. Data Node Linear Average Capacitance Values. Numerical values are given in femtoFarads (fF).

C_{db1}	37.66	C_{GD3}	5.178	C_{db8}	6.82
C_{GD1}	2.62	C_{db5}	17.28	C_{GD8}	2.62
C_{db3}	4.88	C_{GD5}	0.621	C_G	17.26

5.6 Chapter Summary

The design, implementation, and experimental testing of circuits for detection and storage of optical data have been presented in this chapter. The proposed optical data transfer concept has been verified with these circuits. Experimental results were provided for individual storage elements as well as a 4 x 4 array with an external decoding system. The next chapter discusses the extension of optical data transfer technology to other applications.

CHAPTER 6

OPTOELECTRONIC CIRCUIT APPLICATIONS

Transfer of data from a holographic ROM is just one of the many applications for the circuits and concepts presented in this thesis. Some of the other potential applications are discussed in this chapter. The ideas put forth here by no means form an exhaustive list of possibilities that could have been considered. Most of the suggested applications are speculative, and intended mainly for investigation in future research.

Generally, the photonic input to circuits will be called P when the light is on and $\overline{P}$ otherwise. The use of P implies the incident light has the intensity and wavelength necessary to exceed the threshold of the detector circuit. Although P corresponds to the light being on, this does not always imply a logic one. However, when bright true logic is specified, the presence of light implies a logic one and the absence a logic zero. This is particularly useful in describing the optical output of a system.

6.1 Optical Computing

Optical computing has the potential for significant advantages in areas such as speed, reliability, and size when compared to electronic systems. One of the bottlenecks in the field of optical computing is the processing and distribution of data from the output of a parallel computation stage. Assuming such an output is a parallel array of light beams, it can be directly transferred to an electronic RAM using methods described in this thesis and shown in Fig 6-1. The bright true logic scheme can be adhered to, since an optically written logic zero can be applied to either data node of a detection and storage cell.

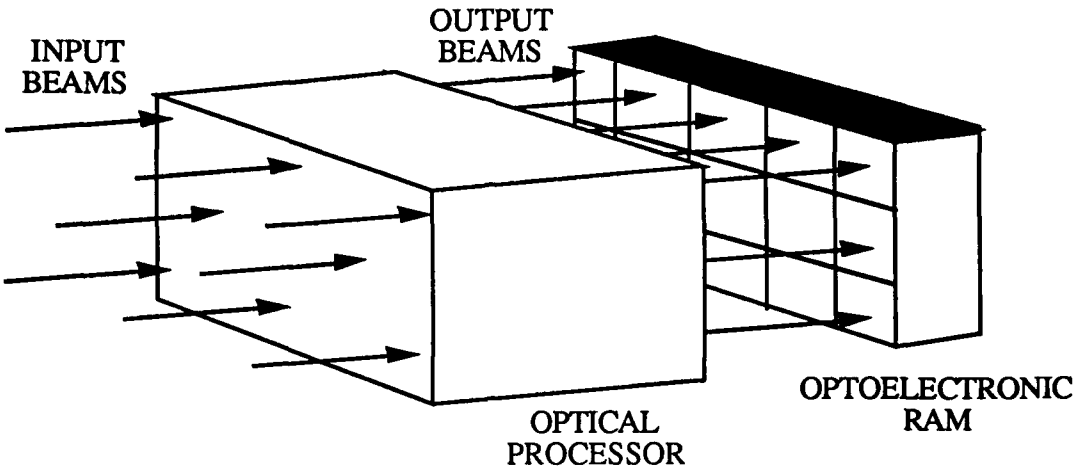


Figure 6-1. Transfer of Optical Output to a Static RAM.

6.1.1 Shadow-Casting Logic

Shadow casting [71, 72] is a means of implementing optical parallel logic gates without the use of lenses. Given two variables A and B, the sixteen logic operations in Table 6-1 can be performed by using masks to code the inputs according to the patterns in Fig. 6-2(a). Superimposing the inputs gives the patterns with one-quarter of each mask transparent as shown in Fig. 6-2(b). The input masks can be illuminated with four LEDs such that the overlapping shadows are cast onto a 3 x 3 screen as shown in Fig. 6-3. The LEDs are arranged such that each casts a shadow on the central square of the output matrix. Illumination of the central square can be expressed as the logic function [73]

$$c = \alpha \bullet (a \bullet b) + \beta \bullet (a \bullet \bar{b}) + \gamma \bullet (\bar{a} \bullet b) + \delta \bullet (\bar{a} \bullet \bar{b}) \qquad (6.1)$$

where c is the output, a and b are the inputs, and α, β, γ, and δ designate the four LEDs. Parallel logic gates can be implemented by using different combinations of inputs and LEDs. All four LEDs need not be used. For example, the NAND function is implemented only with β, γ, and δ.

Table 6-1. Logic Operations Performed with Two Variables.

$F0 = 0$	$F4 = \overline{A} \cdot B$	$F8 = \overline{A+B}$	$F12 = \overline{A}$
$F1 = A \cdot B$	$F5 = B$	$F9 = A \odot B$	$F13 = \overline{A} + B$
$F2 = A \cdot \overline{B}$	$F6 = A \oplus B$	$F10 = \overline{B}$	$F14 = \overline{A \cdot B}$
$F3 = A$	$F7 = A+B$	$F11 = A+\overline{B}$	$F15 = 1$

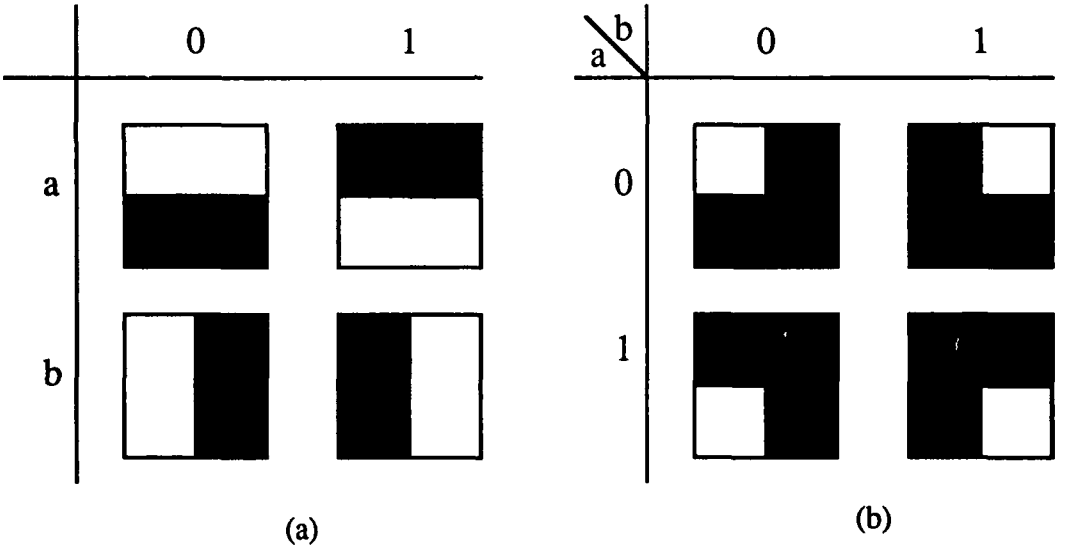


Figure 6-2. Shadow-Casting Logic. (a) Binary inputs. (b) Superimposed inputs. [72]

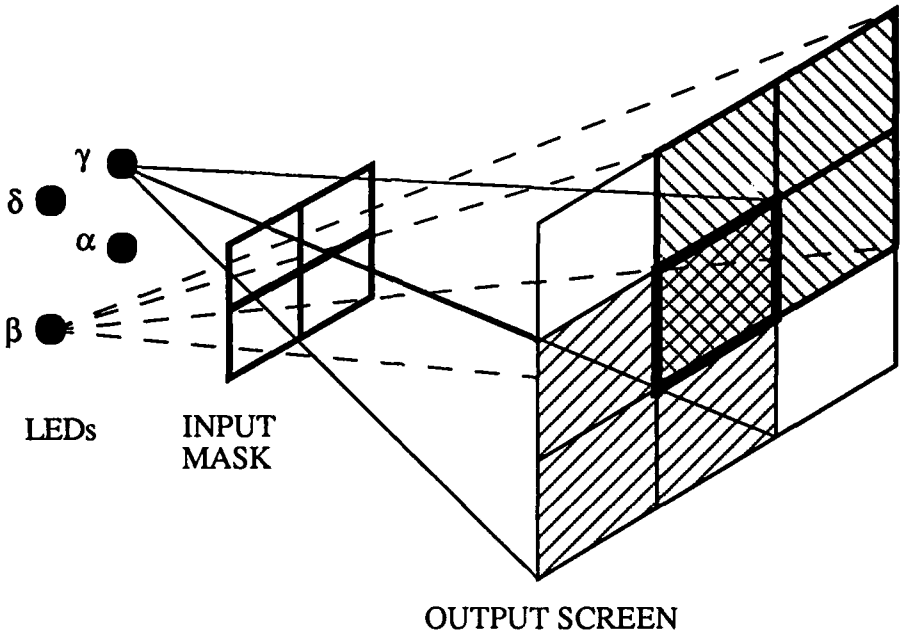


Figure 6-3. Shadow-Casting System. Shadows are shown for two of the four LEDs. All four LED shadows overlap in the center. [72]

A current limitation of shadow casting is the processing of the light beam output of each stage. A potential application for the optical detection and storage system is to receive the output and store the bits for eventual transfer to the next computing process. This can be accomplished simply by developing a mask that blocks out all but the center bit of each gate output screen. The single output beam for each gate is then transferred to a storage cell. Figure 6-4 shows the shadow-casting output screen for an array of 4 logic gates. The required output mask and a 4-bit optical detection and storage cell array are also shown.

6.1.2 Symbolic Substitution Logic

Symbolic substitution logic (SSL) [73-75] is derived from the notion that electronic computers substitute an output for an input when logic operations are performed. A general SSL system is shown in Fig. 6-5. The SSL network must determine the input through a pattern recognition process. It then substitutes the output pattern based on a

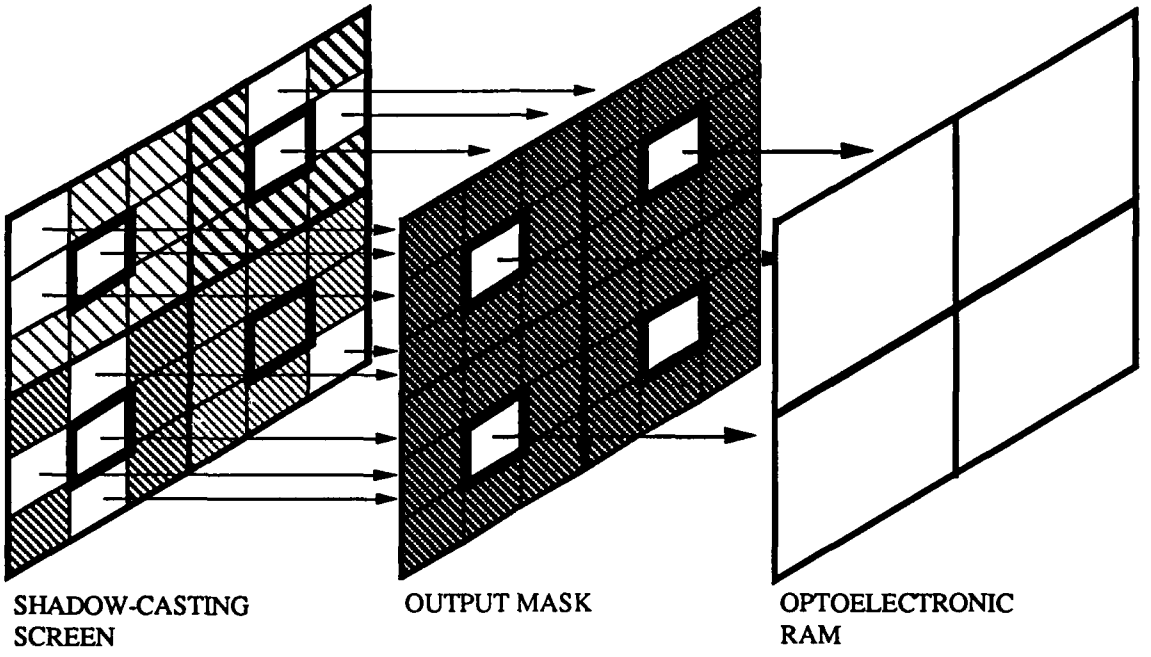


Figure 6-4. Storage of Shadow-Casting Output in an Optoelectronic RAM.

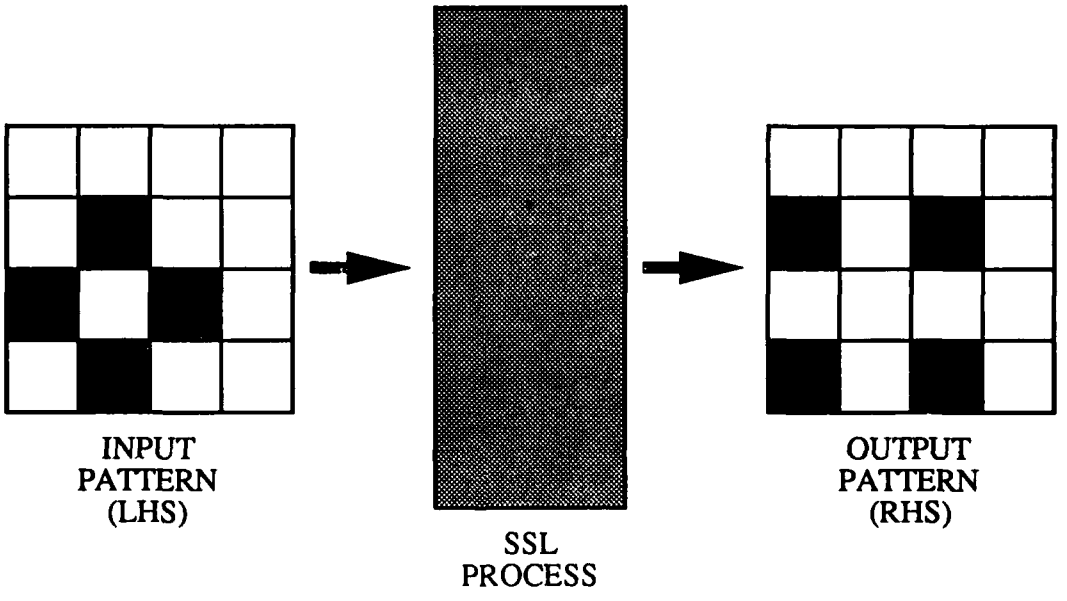


Figure 6-5. Symbolic Substitution Process.

predetermined set of rules, as an electronic computer would perform a logic operation.

An example SSL network is shown in Fig. 6-6. The process starts with the recognition of the pattern. When the input is shifted in four directions, the center is recognized by a high intensity spot. The thresholding device eliminates all other spots and passes the high intensity spot to another shift process. The output pattern is then generated with low intensity spots and passed through a regeneration stage which restores the high intensity to all spots. Rules for SSL, which determine the output for a given input pattern, can be developed to perform the functions of logic gates, computations, and interconnections [73]. The threshold network may be based on the intensity of the bright spot or other parameters such as polarization.

Symbolic substitution logic is another potential application for the optical data transfer concept. The output pattern of an SSL logic system can be transmitted directly to an array of optical detection and storage cells, which gives immediate access to the data

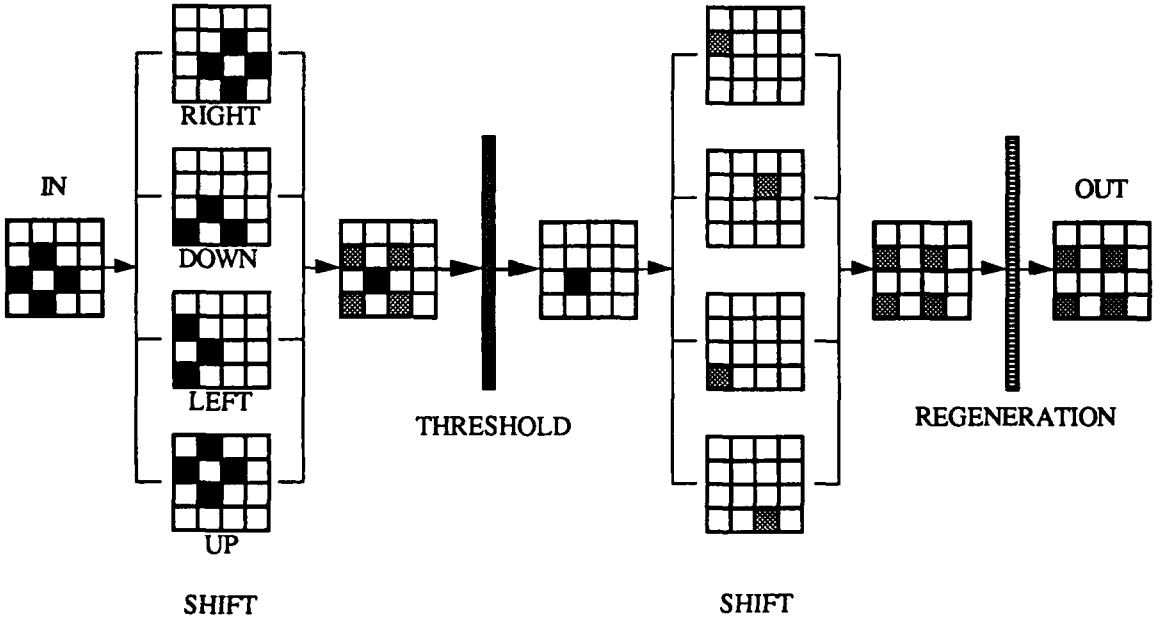


Figure 6-6. Symbolic Substitution Implementation [75].

from a computation. Alternatively, the output may be subjected to other optical processing prior to storage of the new bit pattern.

6.1.3 Multivalued Logic

Multivalued logic [76] allows implementation of functions with fewer inputs. Binary logic offers four possible input combinations to a logic gate and 16 possible output functions. Ternary logic provides nine possible input combinations and performs 19,638 functions [73]. The detector and load circuits in Chapter 4 may offer a third logic state when the response to a photonic input causes the detector output to rise above the supply rail. An example definition for the three states based on the detector output voltage is given in Table 6-2 for a supply rail of 5 volts.

6.2 Optical Fiber Data Transmission

The optoelectronic SRAM presented in Chapter 5 is specifically designed for compatibility with inputs from a holographic ROM. Without major changes, the same system may also accept inputs from an array of optical fibers. Single-mode fibers generally have small cores and a step-index profile between the core and the cladding. Commercially available single-mode fibers have core diameters of 1.5-10 μm and are designed for operating wavelengths in the range of Argon, He-Ne, and other lasers detectable by silicon devices. The fiber cladding and jacket are often 125 μm and 250 μm in diameter, respectively.

Graded-index multimode fibers are inexpensive and easy to work with, but generally have core diameters in the 50-100 μm range. The diameter of the jacket is much larger than that of single-mode fibers, although the cladding diameters are about the same. Ideally, the complete optical fiber fits into a 100 μm square, which is the size of the storage cell. An example system is shown in Fig. 6-7.

Table 6-2. Electronic States for Three Photonic Inputs.

PHOTONIC INPUT	ELECTRONIC STATE	VOLTAGE
$\bar{P}$	0	< 2.5
P	1	2.5 - 5.0
$\hat{\bar{P}}$	$\hat{1}$	> 5.0

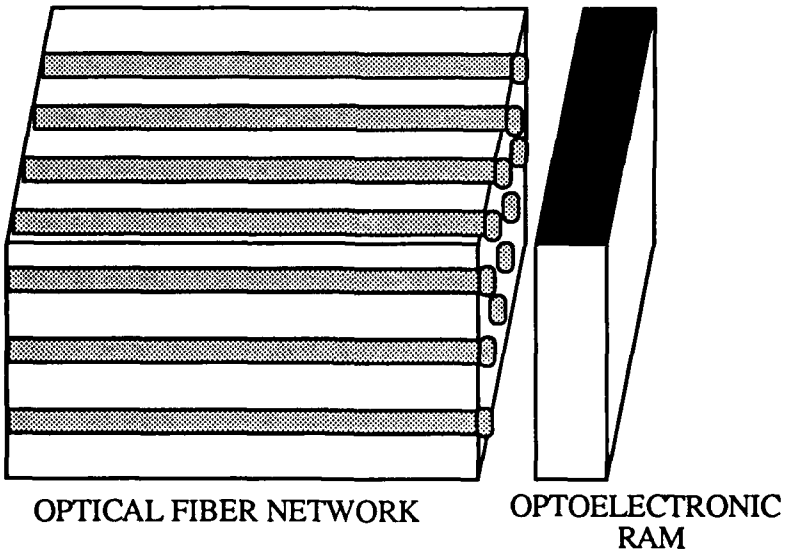


Figure 6-7. Optoelectronic Static RAM with Input from Optical Fibers.

6.3 Optically Reconfigurable Logic

Figure 6-8 shows an example of a combinational logic circuit reconfigured by an optical input. When P = 0, the output of the circuit is the AND-OR-INVERT shown in Fig. 6-8(b). Application of the optical input switches the logic expression to the OR-AND-INVERT in Fig. 6-8(c). If b = a and c = d, P = 1 creates an XOR operation on inputs a and d. The NMOS transistor controlled by the optical circuit includes body bias effects and causes the circuit to deviate from the complementary operation for which it was designed. The optical input could have also been placed in parallel with one of the existing inputs.

6.4 Optical Inputs to CMOS Logic Gates

The detector circuits in Chapter 4 may be used as inputs to logic circuits to obtain an electronic output from either all optical inputs or a combination of electronic and optical input variables. Figure 6-9 shows a CMOS NAND gate with an optical input and an electronic input. This type of circuit could be a basis for a simple optical processor. An optical processor using photonic inputs may be controlled by a volume hologram or an optical fiber network.

6.5 Optically-Controlled Circuits

A fundamental optical control circuit is shown in Fig. 6-10. Under dark conditions, P is set to a logic zero. Control applications include logic circuits, interconnects, address encoders and decoders, and pass transistors. Figure 6-11 is a simple 2 x 1 multiplexer realized from two transmission gates and controlled optically. This circuit has been selected to demonstrate this principle because it can be easily expanded to larger multiplexer circuits. It also performs logic operations on the optical control parameters and the input variables according to the input table accompanying the figure. A single transmission gate may also be used in the applications listed above.

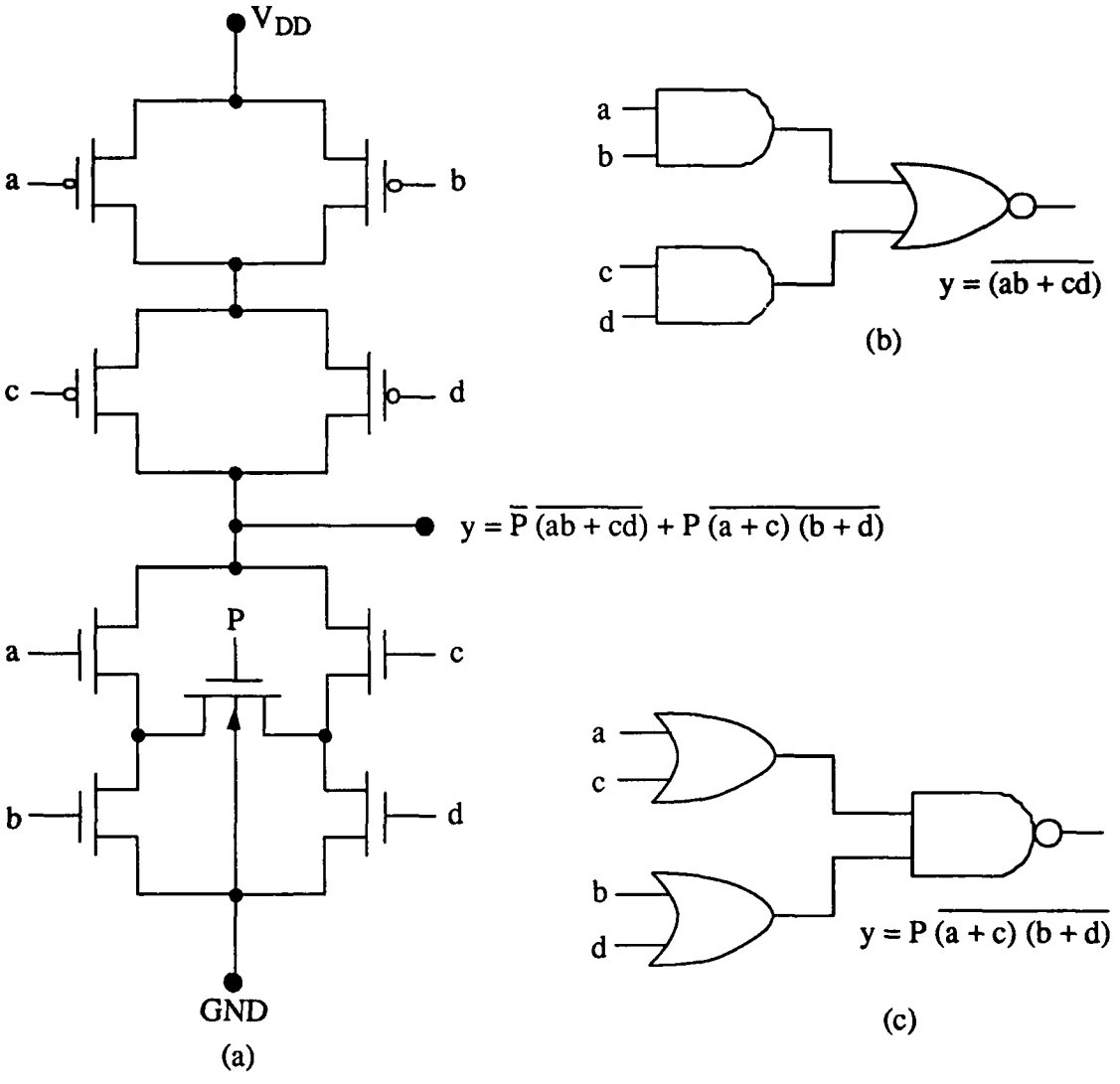


Figure 6-8. Optically-Reconfigured Circuit. (a) Schematic diagram. (b) Gate equivalent without optical input. (c) Gate equivalent with optical input.

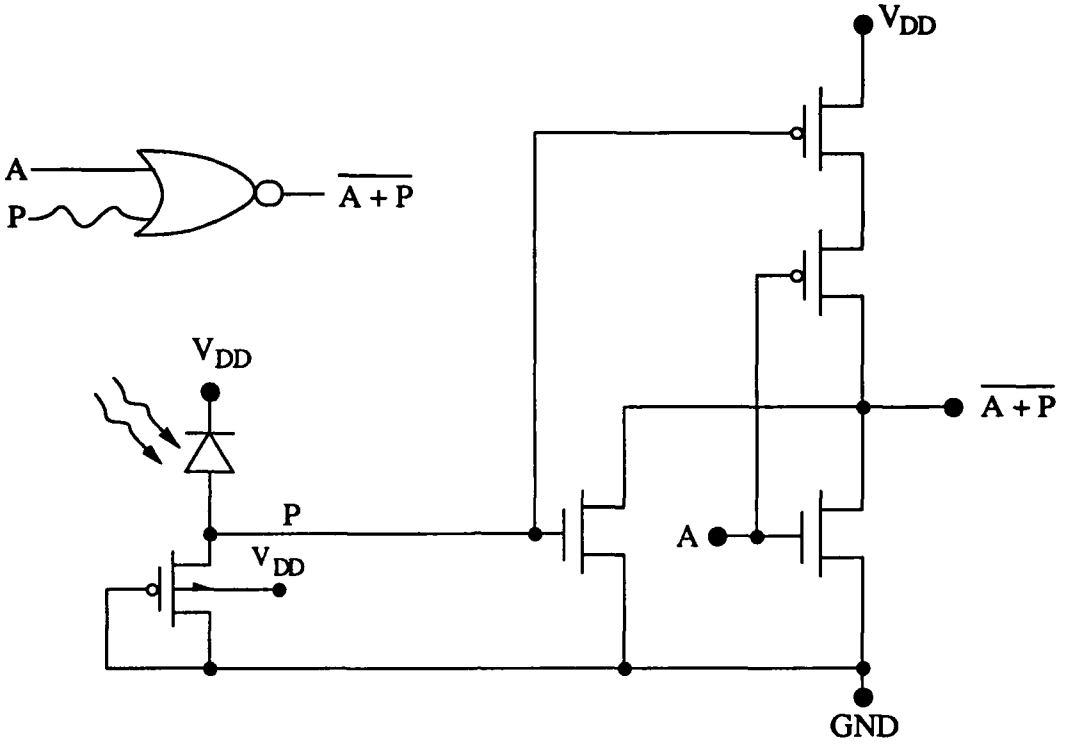


Figure 6-9. NAND Gate with Optical Input.

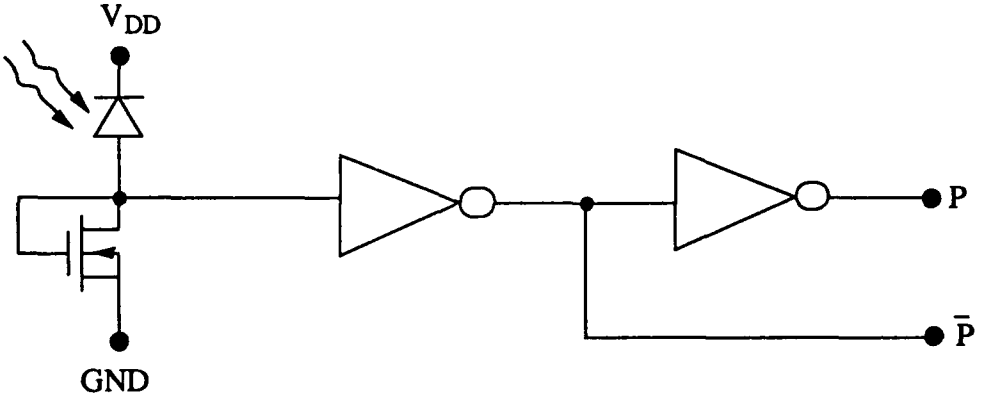
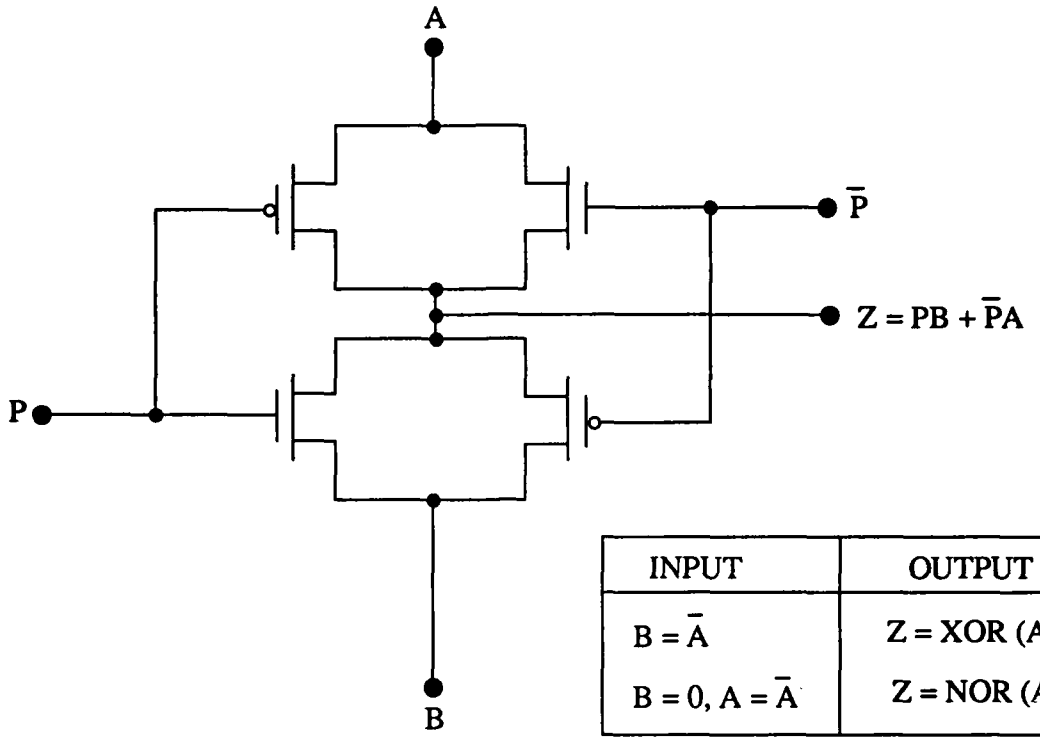


Figure 6-10. Optical Control Circuit.



INPUT	OUTPUT
$B = \bar{A}$	Z = XOR (A, P)
$B = 0, A = \bar{A}$	Z = NOR (A, P)

Figure 6-11. Optically-Controlled Circuit for Multiplexing and Logic Operations.

6.6 State-of-the-Art Memories

Portions of the optical data transfer system may be applicable to new approaches to optical storage and optical readout of data. Associative or content-addressable memories [77] are based on the storage of data in the pages of a volume hologram. Readout from the memory is accomplished by using part of the stored pattern to illuminate the hologram. As a result, the reference beam that corresponds to that pattern is reconstructed. Once the appropriate reference beam has been identified, it is reproduced to read out the whole data page. This approach to data storage is similar to optical ROM-to-electronic RAM data transfer. Thus, during the readout of the associative memory, the data can be transferred to an array of optical detection and storage cells.

Another process which may apply to the optical data transfer technology is optical multiprocessor interconnects (OPTIMUL) [78]. This concept proposes the parallel readout of data from a standard electronic memory by an array of reflected light beams. The data storage locations in the memory are coated with a thin polymeric film. When the nodes are illuminated, the electric field where data is stored causes intensity modulation of the incident light. The reflected beam then contains a bit map of the contents of the accessed RAM. The OPTIMUL system proposes simultaneous transfer of the contents of the reflected beam to several processors using photodetector technology. Instead, the data could be transferred to multiple optoelectronic static RAMs which are associated with the processors. Another alternative is to modify the optical detection and storage cell array in Chapter 5 to allow readout using the OPTIMUL system. This would create a memory with parallel optical write and parallel optical read. A diagram of an OPTIMUL system is shown in Fig. 6-12.

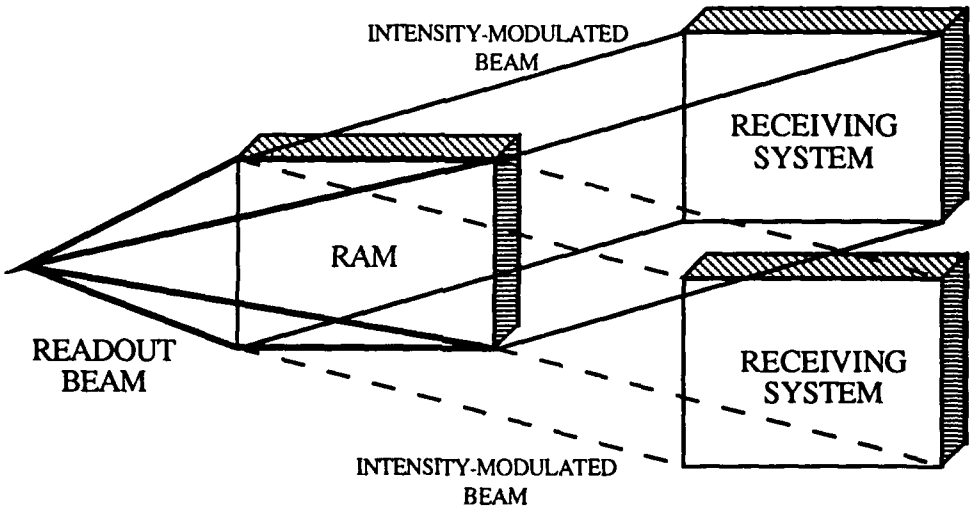


Figure 6-12. Optical Multiprocessor Interconnect System.

CHAPTER 7

CONCLUSIONS

7.1 Summary of Results

A system for parallel detection and storage of optically transmitted data has been designed, fabricated, and tested. Development of the circuits for receiving data contained in a parallel array of low power light beams was based on the examination of topics in several different areas. A graphical approach to CMOS SRAM cell design that provided a basis for determining the interaction between the optical and electronic circuits was introduced. The theoretical and experimental performance of photodetection devices fabricated in a bulk CMOS process was presented. A number of detector load devices were compared on a theoretical and experimental basis to determine suitability for conversion of optical signals to a DC voltage. Finally, a RAM cell was developed for detection and static storage of data transferred from a holographic ROM.

7.1.1 Design of CMOS Static RAM Cel

A stability analysis of a CMOS static RAM cell was performed using basic transfer characteristics of MOSFET inverters. The analysis was based on the retention of data during the worst-case read operation. A static RAM cell storing a logic zero is most susceptible to noise when the information at the DATA node is transferred through an access transistor to the BIT line. Soft errors occur because the read operation temporarily raises the voltage at the DATA node. Under normal conditions, the change in voltage is inadequate to cause the stored bit to change to a logic one. However, when noise from a variety of sources is added, the net change in DATA node voltage may cause a random soft

error or a change of data. The size of the cell noise margin determines the immunity of the cell to noise. Three fundamental parameters were used for the analysis. The CMOS inverter threshold determines the point at which a transition from a logic one to a logic zero occurs. The CMOS inverter input low voltage is the maximum logic zero input that assures a logic one at the output. This parameter represents the allowable change in voltage at the DATA node, including noise. The third parameter is the output low voltage of an NMOS inverter, which determines the change in voltage at the DATA node during a read operation. These three parameters were displayed graphically and then combined to obtain a low noise margin. It was shown that the results from this analysis are supported by a published static noise margin calculation. This work has three important features. For a range of transistor aspect ratios, it serves the same purpose as the static noise margin, but is much less complex and offers better insight into the operation of the cell. Second, a version of the static noise margin was derived for fabrication processes in which the PMOS and NMOS thresholds are of different magnitudes. Finally, this approach to cell design translates directly into a method for determining the interaction between the basic SRAM cell and the optical circuit addition.

7.1.2 Silicon Integrated Photodetection Devices

A geometry was presented for several silicon photodetection devices that are compatible with CMOS fabrication processes. The pn junction photodiode was used as a basis for analysis of these shallow-junction devices. Two large signal models for SPICE simulations were developed from the diode equivalent circuit. An established averaging method was applied to the diode capacitance and depletion layer width. The photodetection process and each component of the photon-generated current were analyzed in terms of special considerations for shallow-junction devices. As a result, alternatives to the standard expression for photocurrent were presented. Two complete models were given for

photodiodes fabricated in a bulk CMOS process. The respective model parameters were tabulated for easy application to optoelectronic circuits.

7.1.3 Detection of Optical Data

Load devices for the shallow-junction photodetectors were examined. The devices were restricted to n-channel and p-channel MOSFETs biased in the three different regions of operation. Both pull-up and pull-down circuits were considered. The detectors with load devices were compared in terms of theoretical performance as well as simulation and experimental results. Two load device configurations were found to be acceptable for low power optical input applications. Based on this analysis, an empirical value for the effective fast surface state density model parameter was proposed.

7.1.4 Storage of Optically Transmitted Data

The most important portion of the research was accomplished in this area. A 16-bit memory was developed for detection and storage of optically transmitted data. Circuits for optically writing information to a storage node were developed and added to a CMOS static RAM cell, which was designed specifically for optical applications. The theoretical transient behavior of the cell and the possibility of undesirable interaction between the optical and electronic components were examined. The cells were geometrically arranged for compatibility with input in the form of a parallel array of light beams from a volume hologram. The presence of light at a particular location in the cell was interpreted to be transmission of a logic zero. The absence of light having the minimum threshold intensity was considered to be a logic one.

The memory was fabricated in a p-well, CMOS process. The layout was based on 2 μm scalable CMOS rules. The optoelectronic RAM cells were tested individually and collectively for optical data storage and electrical data storage and retrieval. Several different bit patterns were used to test the parallel write capability of the 16-bit RAM.

Successful tests were performed using light patterns formed by a series of optical masks placed in the path of an Argon laser beam. The concept of parallel optical data transfer was also verified by using an array of light beams from the output of a hologram. The results given in this section are important to the research on optical ROM-to-electronic RAM data transfer. The primary application is parallel transmission of a secure instruction set to a processor.

7.2 Recommendations for Future Research

Two areas exist for potential continuation of the research presented in this thesis. One area is associated with the ongoing research of optical ROM-to-electronic RAM data transfer. The other potential research concerns improvements to the optical detection and storage cell and extensions of the optical data transfer technology to other applications.

7.2.1 Optical ROM-to-Electronic RAM Data Transfer

Develcpment of the volume hologram for the optical ROM-to-electronic RAM data transfer system is in progress. The next phase of the electronics part of the research is a 256-bit RAM with on-chip decoders and output circuits. The RAM is currently in fabrication. Preparations are also being made for experimental determination of the time interval for the optical write process.

7.2.2 Optical Detection and Storage Cell

Although not vital to the completed phase of the optical data transfer research, the transient response of individual photodetectors is in need of further attention. Investigation of this topic would contribute to the optical ROM-to-electronic RAM technology, as well as many other areas such as optical computing and optical interconnects. The transient response of detectors is particularly important for silicon systems using light sources of longer wavelengths (e.g. 0.8-1.0 μm). The low absorption coefficient of such light

sources causes a large number of carriers to be generated in the substrate.

The optical portion of the detection and storage cell may be considered for further examination. The development of innovative load devices and current amplifiers may reduce the capacitance seen by the detector and speed up the write operation. At the same time, the optical power may be reduced.

The optical detection and storage cell may eventually need to be reduced in size. The impact of fabricating the circuit in a 0.6, 0.8, or 1.2 μm process must be determined. Future research should also consider other ways to accomplish the same optical write process.

APPENDIX A

CIRCUIT LAYOUT AND FABRICATION

An important part of research is the opportunity to fabricate circuits and obtain experimental support of theoretical concepts. Thus far, eight *tinychips* have been fabricated in support of research related to optical ROM-to-electronic RAM data transfer. The *tinychip* is a name given to a small, low-cost chip available through the MOSIS. This appendix details the layout and fabrication of chips used to support this work.

A.1 Circuit Layout

The MAGIC graphical editor was used to create the layout for each of the chips fabricated. All layouts were developed on a Sun-160 work station with an integrated color display. The MOSIS Scalable CMOS design rules were used to generate the layouts, with the scale parameter λ set to a value of 1.0 as required for the 2 μm fabrication process. The minimum transistor dimensions were 3 μm and 2 μm for the channel width and length, respectively. Each layout was converted to Caltech Intermediate Form (CIF) format and submitted to the MOSIS via electronic mail.

A.2 Fabrication Process

All chips were fabricated in a 2 μm CMOS/bulk process which offered two layers of metal and polysilicon. P-wells were specified due to the photosensitive regions in the circuit. An example *tinychip* pad frame with a 16-bit RAM is shown in Fig. A-1. Model parameters were provided for each chip fabricated at the MOSIS. Parameters averaged over an eight month period are given in Table A-1.

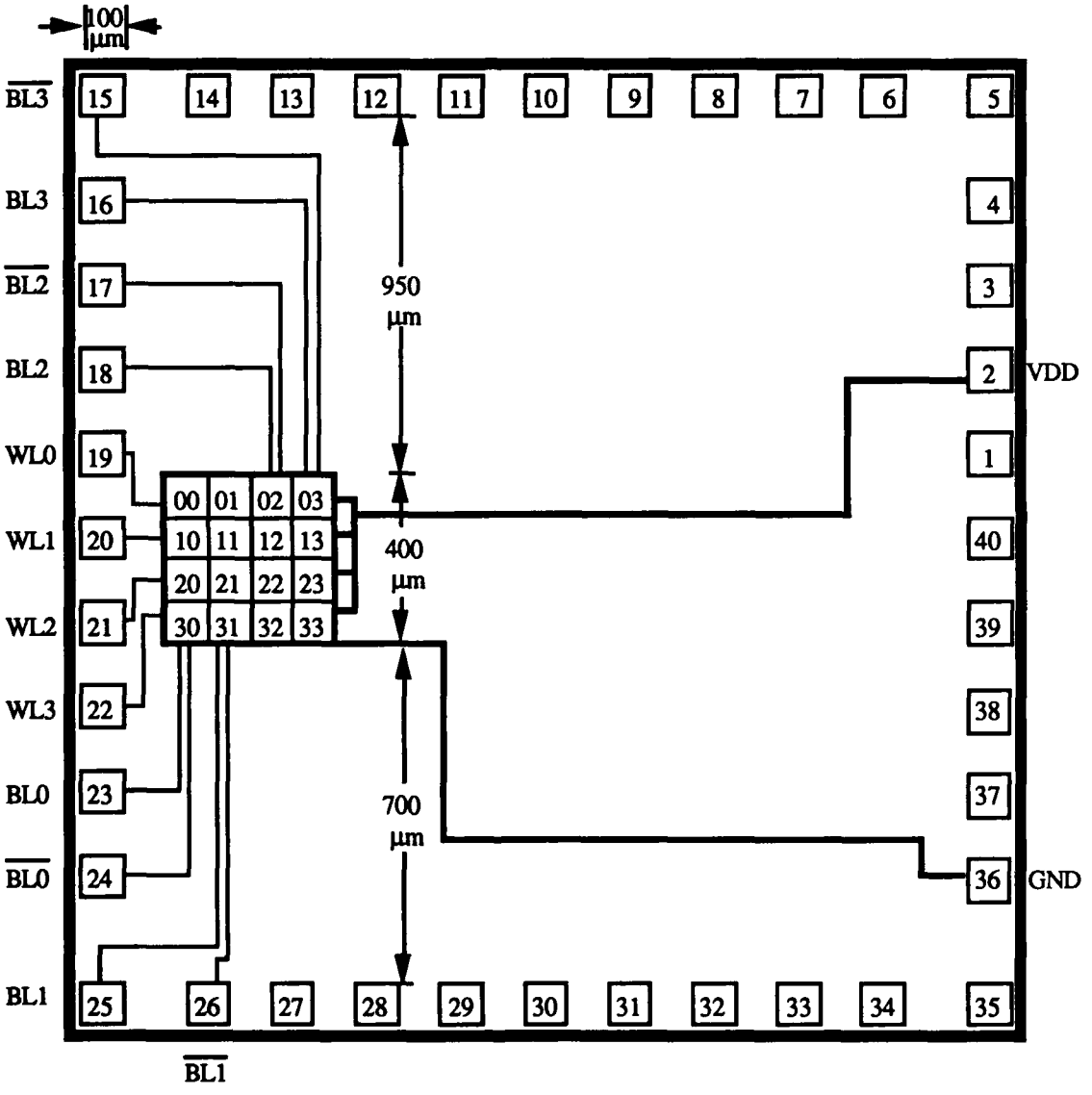


Figure A-1. Example of a Tinychip Pad Frame. The chip is 2200 µm wide and 2250 µm long. Bonding pads not connected to the memory array were used for individual photodetectors, detector load circuits, and optical write circuits.

Table A-1. SPICE Model Parameters. Parameters are average values extracted from three fabrication runs over an eight month period.

PARAMETER	UNITS	NMOS	PMOS
LEVEL	--	2.00	2.00
VTO	V	1.00	-0.74
KP	A/V^2	55.100E-6	21.80E-6
GAMMA	$V^{0.5}$	1.01	0.49
PHI	V	0.60	0.60
LAMBDA	1/V	2.37E-2	5.76E-2
DELTA	--	1.51	1.46
XJ	M	0.25E-6	0.25E-6
CGSO, CGDO	F/M	3.18E-10	3.11E-10
CJ	F/M^2	3.97E-4	1.94E-4
MJ	--	0.46	0.43
CJSW	F/M	5.15E-10	2.55E-10
MJSW	--	0.36	0.28
TOX	M	40.00E-9	40.00E-9
LD	M	0.24	0.24
NSUB	CM^{-3}	2.27E16	5.48E+14
UEXP	--	0.24	0.24
UCRIT	V/CM	11.64E+4	50.39E+3
VMAX	M/S	86.40E+3	43.00E+3
NFS	CM^{-2}	2.26E+12	3.093+11
NEFF	--	1.00	1.00
NSS	CM^{-2}	1.00E+12	1.00E+12
TPG	--	1.00	-1.0
RSH	Ω/SQ.	21.04	72.06
PB	V	0.8	0.70
CGBO	F/M	6.94E-10	6.66E-10

APPENDIX B

EXPERIMENTAL SETUP

In the equipment arrangement in Fig. B-1, two 10X microscope objectives are used to focus the Helium-Neon laser beam into and out of a spatial filter with a 15 μm pinhole. The beam is then projected onto the test chip via two mirrors, a 10X eyepiece, and a 10X microscope objective. Micro positioners are used to adjust the microscope objectives to achieve a minimum spot size at the location of the test chip. With the chip carrier in a fixed position and the beam focused on a photodetector, the microscope objectives and mirrors are further adjusted to obtain maximum photocurrent.

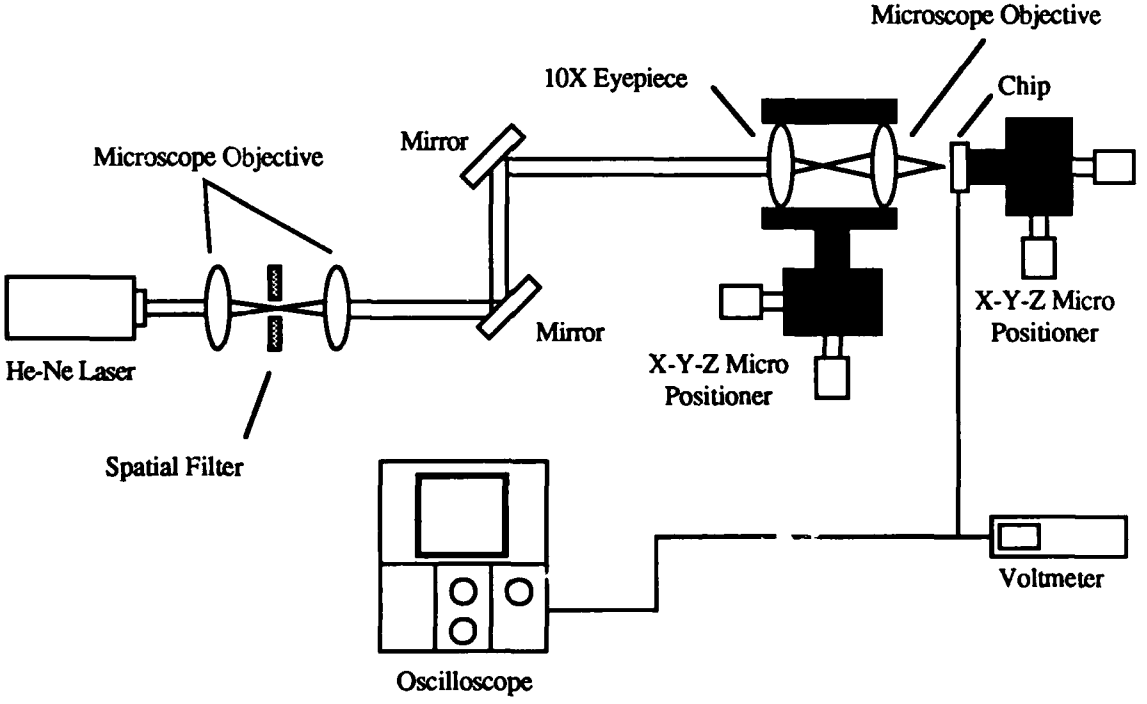


Figure B-1. Experimental Setup for Laboratory Measurements.

During experimental measurements, the optical equipment must remain in the properly aligned position. The relative locations of the light beam and the test chip are controlled by a micro positioner on which the chip carrier is mounted. The positioner for the 10X microscope objective and eyepiece is mounted on a laboratory jack, but remains stationary once proper alignment has been obtained. The positioner for the chip carrier is mounted on an optical rail, which restricts the motion of the chip to only the movement of the micro positioner. A beam splitter/attenuator is used to vary the intensity of light incident on the chip. The incident light power is measured with a power meter. Measurements are taken by temporarily placing the meter in front of the 10X eyepiece and adjusting the position until the maximum reading is obtained. A photograph of the laboratory equipment is shown in Fig. B-2 and listed in Table B-1.

The response of two photodiodes to a vertical scan of the laser beam is shown in Fig. B-3. Detector A is a p^+n^- photodiode with the p^+ implant 46 μm long in the direction of

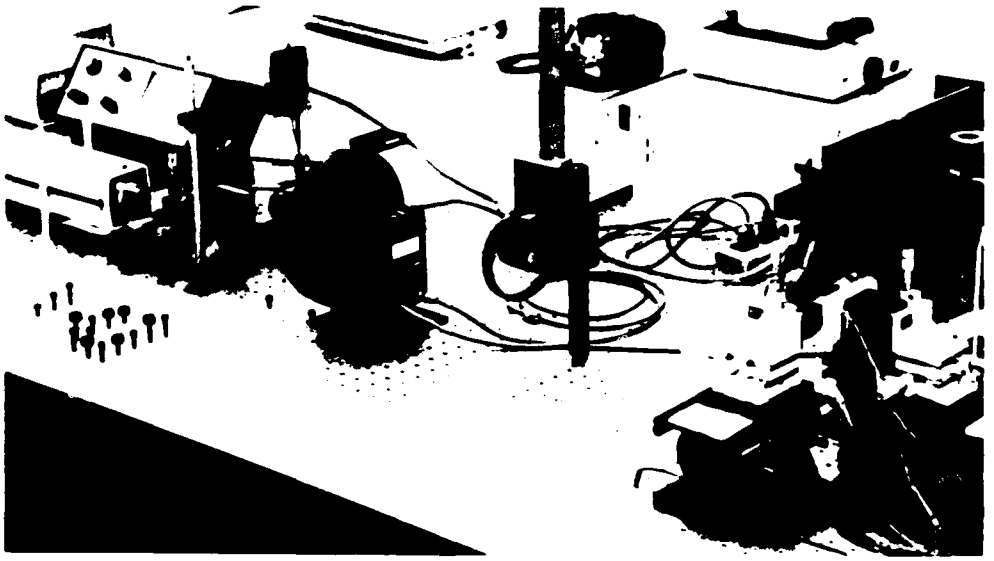


Figure B-2. Photograph of Laboratory Equipment Used for Experimentation.

Table B-1. List of Basic Equipment Used for Experiments

Spectra Physics Model 155 Helium-Neon Laser (0.95 mW maximum output)	Oscilloscope Tektronix 5103N - 5A18N Dual Trace Amplifier
Spectra Physics Model 124B Helium-Neon Laser (15 mW maximum output)	Probe/Test Station
Beam Folding Mirror and Mount (2)	Jodon VBA-200 Beam Splitter
Coherent Model 212 Power Meter	HP 3476A DMM
X-Y-Z Micro Positioner (3)	Unidirectional Positioner (2)
10X Eyepiece	10X Microscope Objective (3)
	Spatial Filter

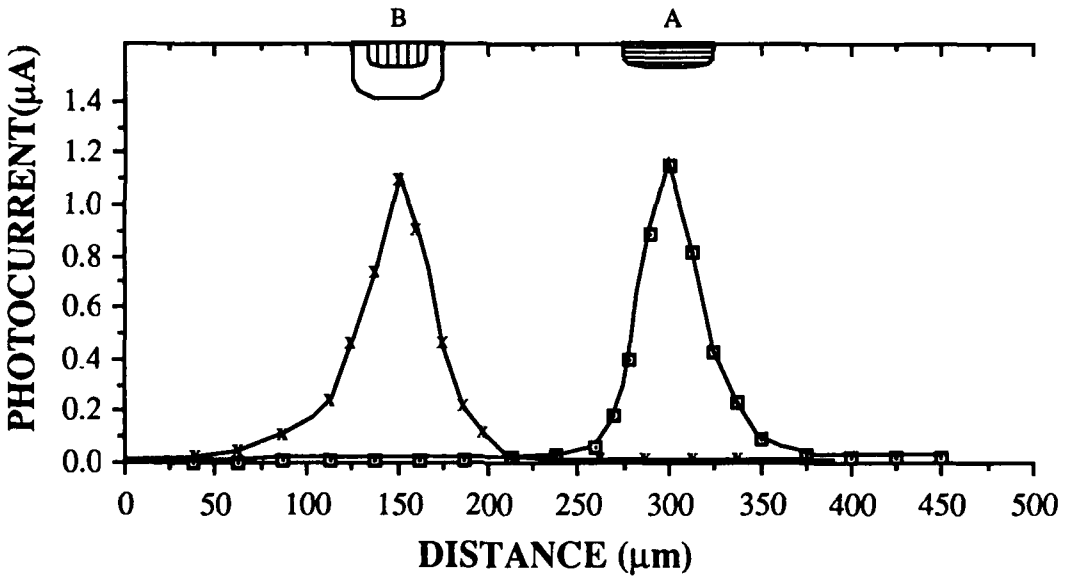


Figure B-3. Response of Two Photodiodes to a Laser Beam Scan.

the scan. Detector B is an n^+pn^- device with both n-type regions connected to the positive supply voltage. The n^+ implant is 32 μm in the scan direction, while the p-well is 50 μm long. The spacing between detector centers is 147 μm. From the valley in the figure and the known spacing of 108 μm between the edges of the photosensitive regions, the spot size is estimated to be in the range of 30-45 μm.

APPENDIX C

EXAMPLE SPICE INPUT FILES

The SPICE circuit simulator was used throughout the research to support theoretical calculations and predict experimental results. Generally, the simulations were run on a personal computer. In some cases PSPICE was used. The sample input files are given in the next paragraphs.

C.1 Simulation of a Photodiode and NMOS Load

```
NONSAT NFET LOAD
VDD 2 0 5

IP 2 1 PWL(0 0 5N 0 6N 40U 106N 40U 107N 0)

*DIODE MODEL IS FOR AREA OF 30X30
D1 1 2 DMOD 1
.MODEL DMOD D(IS=0.718E-14 RS=100 TT=0.1N CJO=81F VJ=0.86)

M1 1 2 0 0 NMOD L=20U W=3U AD=20P AS=20P PD=20U PS=20U
.MODEL NMOD NMOS(LEVEL=2 LD=0.24U TOX=400E-10 NSUB=2.27E+16
+VTO=1 KP=5.51E-5 GAMMA=1.01 PHI=0.6 UO=616.32 UEXP=0.24
+UCRIT=116400 XJ=0.25U LAMBDA=2.37E-2 NFS=2.26E+12 NEFF=1 NSS=1E+12
+TPG=1 RSH=21.04 CGDO=3.18E-10 CGSO=3.18E-10 CGBO=6.94E-10 CJ=3.97E-4
+MJ=0.46 CJSW=5.15E-10 MJSW=0.36 PB=0.8 DELTA=1.51 VMAX=86400)
.MODEL PMOD PMOS(LEVEL=2 LD=0.24U TOX=400E-10 NSUB=5.48E+15
+VTO=-0.74 KP=2.18E-5 GAMMA=0.49 PHI=0.6 UO=271.78 UEXP=0.24
+UCRIT=50392 XJ=0.25U LAMBDA=5.76E-2 NFS=3.09E+13 NEFF=1 NSS=1E+12
+TPG=-1 RSH=72.06 CGDO=3.11E-10 CGSO=3.11E-10 CGBO=6.66E-10
+CJ=1.94E-4 MJ=0.43 CJSW=2.55E-10 MJSW=0.28 PB=0.7 DELTA=1.46
+VMAX=43000)

.TRAN 5N 200N
.PRINT TRAN V(1) ID(M1) I(D1) I(IP)
.PROBE V(1) ID(M1) I(D1) I(IP)
.END
```

C.2 Simulation of an Optoelectronic SRAM Cell

```
TRANSIENT RESPONSE FOR OPTICAL WRITE
VDD 5 0 5
```

```
IP 5 8 PWL(0 0 5N 0 6N 10U 106N 10U 107N 0)

.NODESET V(2)=5
.OPTIONS NOMOD ITL1=300 ITL2=300

VBL 1 0 5
VBLN 4 0 5
VWL 7 0 0
VWLN 6 0 0

*DIODE MODEL IS FOR AREA OF 30X30
D1 8 5 DMOD 0.28
.MODEL DMOD D(IS=1.218E-14 RS=100 TT=0.1N CJO=81F VJ=0.86)

M1 2 3 0 0 NMOD L=2U W=4U AD=28P AS=64P PD=28U PS=34U
M2 3 2 0 0 NMOD L=2U W=4U AD=28P AS=20P PD=22U PS=18U
M3 2 3 5 5 PMOD L=4U W=3U AD=23P AS=22P PD=20U PS=20U
M4 3 2 5 5 PMOD L=4U W=3U AD=23P AS=22P PD=20U PS=20U
M5 1 7 2 0 NMOD L=4U W=3U AD=22P AS=60P PD=46U PS=20U
M6 4 6 3 0 NMOD L=4U W=3U AD=22P AS=60P PD=46U PS=20U
M7 0 0 8 5 PMOD L=30U W=3U AD=16P AS=16P PD=20U PS=20U
M8 2 8 0 0 NMOD L=2U W=4U AD=28P AS=64P PD=28U PS=34U

.MODEL NMOD NMOS(LEVEL=2 LD=0.24U TOX=400E-10 NSUB=2.27E+16
+VTO=1 KP=5.51E-5 GAMMA=1.01 PHI=0.6 UO=616.32 UEXP=0.24
+UCRIT=116407 XJ=0.25U LAMBDA=2.37E-2 NFS=2.26E+12 NEFF=1 NSS=1E+12
+TPG=1 RSH=21.04 CGDO=3.18E-10 CGSO=3.18E-10 CGBO=6.94E-10 CJ=3.97E-4
+MJ=0.46 CJSW=5.15E-10 MJSW=0.36 PB=0.8 DELTA=1.51 VMAX=86404)

.MODEL PMOD PMOS(LEVEL=2 LD=0.24U TOX=400E-10 NSUB=5.48E+15
+VTO=-0.74 KP=2.18E-5 GAMMA=0.49 PHI=0.6 UO=271.78 UEXP=0.24
+UCRIT=50392 XJ=0.25U LAMBDA=5.76E-2 NFS=3.09E+11 NEFF=1 NSS=1E+12
+TPG=-1 RSH=72.06 CGDO=3.11E-10 CGSO=3.11E-10 CGBO=6.66E-10
+CJ=1.94E-4 MJ=0.43 CJSW=2.55E-10 MJSW=0.28 PB=0.7 DELTA=1.46
+VMAX=42999)

.TRAN 5N 200N
.PRINT TRAN V(1) V(2) V(3) V(4) V(6) V(7) I(D1) IS(M7) I(IP)
.PROBE V(2) V(3) V(8) ID(M8) ID(M1) ID(M3) I(D1) IS(M7) I(IP)
.END
```

C.3 Determination of Transistor Characteristics

```
SAT PFET LOAD
VSD 1 0 0
VDD 2 0 5

M2 0 0 1 2 PMOD L=2U W=3U AD=20P AS=20P PD=20U PS=20U
M3 0 0 1 2 PMOD L=3U W=3U AD=20P AS=20P PD=20U PS=20U
M4 0 0 1 2 PMOD L=10U W=3U AD=20P AS=20P PD=20U PS=20U
```

```
M5 0 0 1 2 PMOD L=20U W=3U AD=20P AS=20P PD=20U PS=20U
M6 0 0 1 2 PMOD L=30U W=3U AD=20P AS=20P PD=20U PS=20U

.MODEL NMOD NMOS(LEVEL=2 LD=0.24U TOX=400E-10 NSUB=2.27E+16
+VTO=1 KP=5.51E-5 GAMMA=1.01 PHI=0.6 UO=616.32 UEXP=0.24
+UCRIT=116400 XJ=0.25U LAMBDA=2.37E-2 NFS=0.56E+12 NEFF=1 NSS=1E+12
+TPG=1 RSH=21.04 CGDO=3.18E-10 CGSO=3.18E-10 CGBO=6.94E-10 CJ=3.97E-4
+MJ=0.46 CJSW=5.15E-10 MJSW=0.36 PB=0.8 DELTA=1.51 VMAX=86400)

.MODEL PMOD PMOS(LEVEL=2 LD=0.24U TOX=400E-10 NSUB=5.48E+15
+VTO=-0.74 KP=2.18E-5 GAMMA=0.49 PHI=0.6 UO=271.78 UEXP=0.24
+UCRIT=50392 XJ=0.25U LAMBDA=5.76E-2 NFS=3.09E+13 NEFF=1 NSS=1E+12
+TPG=-1 RSH=72.06 CGDO=3.11E-10 CGSO=3.11E-10 CGBO=6.66E-10
+CJ=1.94E-4 MJ=0.43 CJSW=2.55E-10 MJSW=0.28 PB=0.7 DELTA=1.46
+VMAX=43000)

.DC VSD 0 5 0.2
.PRINT DC V(1) IS(M2) IS(M3) IS(M4) IS(M5) IS(M6)
.PROBE V(1) IS(M2) IS(M3) IS(M4) IS(M5) IS(M6)
.END
```

APPENDIX D

SRAM CELL ARRAY READOUT CIRCUIT

A static RAM is generally arranged for individual access of each cell for readout of data. The BIT lines run vertically and are connected to every cell in a column via access transistors. Only a single bit of data can be placed on a BIT line at one time. The word lines run horizontally and access all transistors in a row at once. All of the data from the RAM cannot be displayed at the same time. The most data that can be read at once is a complete row. To read the entire RAM, the rows must be accessed sequentially by turning the word lines on and off.

Using commercially available integrated circuit chips, a readout circuit was designed and built for the 4 x 4 array of optical detection and storage cells. A two-position switch was connected to each of the word lines to allow connection to either 5 volts or ground. Switches were also connected to the BIT lines and NOT BIT lines to allow each one to either be connected to ground or left floating. These two positions were required for electrical write and read operations, respectively. The readout circuit in Fig. D-1 is connected to the BIT and NOT BIT lines through a set of on-off switches. The stage after the switches is a comparator which functions as a sense amplifier to detect and latch the voltage difference of the BIT and NOT BIT lines. Four CMOS NAND gates are then used to accommodate the word line inputs for each BIT line and identify the cell being addressed. The output of each NAND gate goes to an inverting buffer which acts as an interface between CMOS and TTL. Each buffer drives the base of a bipolar transistor. These devices each drive one of the 16 LEDs, which correspond to the 16 RAM cells.

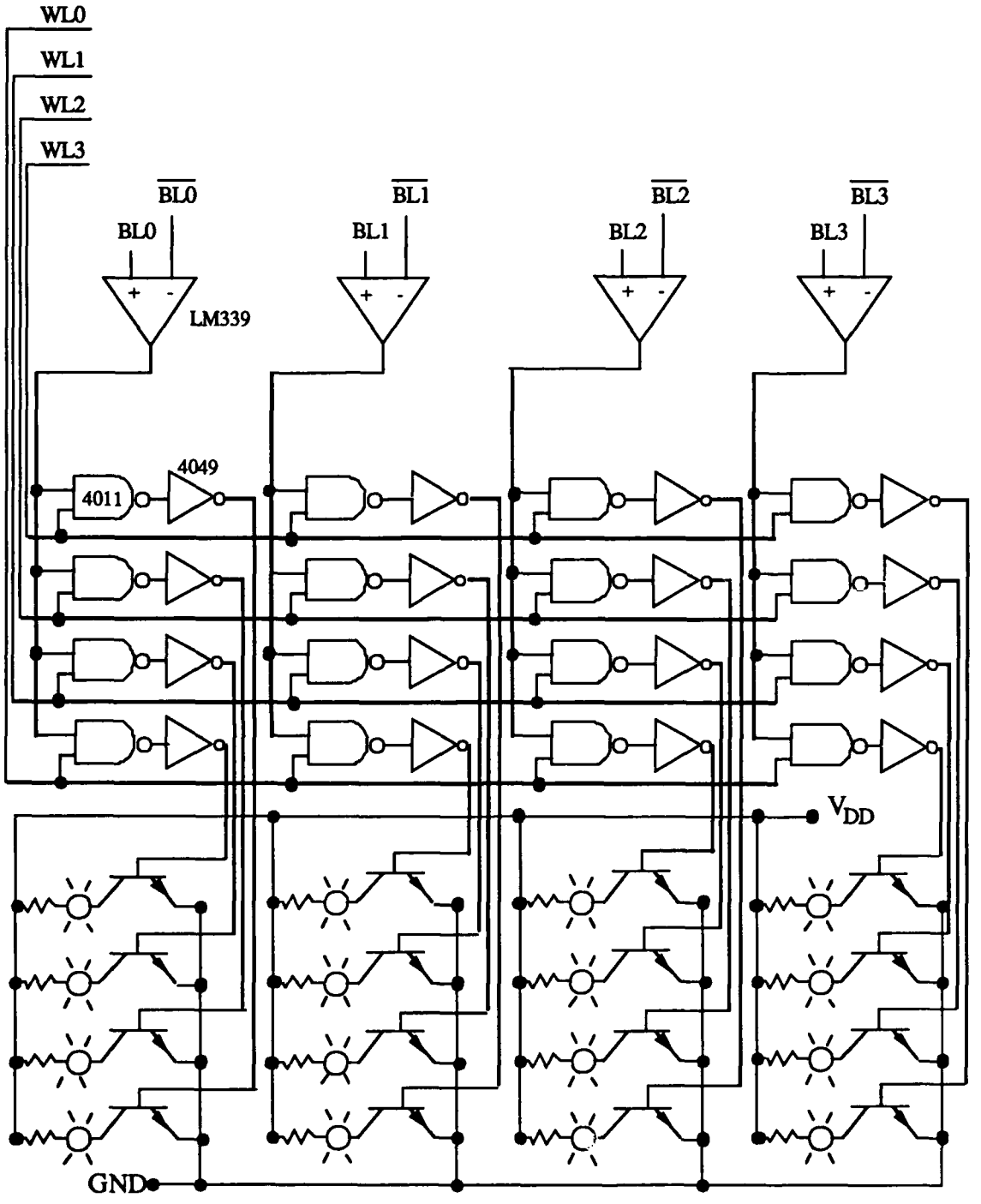


Figure D-1. SRAM Readout Circuit.

REFERENCES

[1] J. Fried, "Optical I/O for high speed CMOS systems," *Opt. Engr.*, vol. 25, pp. 1132-1141, Oct. 1986.

[2] R. W. Keyes, "Fundamental limits in digital information processing," *Proc. IEEE,* vol. 69, pp. 267-278, Feb. 1981.

[3] K. Saraswat and F. Mohammadi, "Effect of scaling of interconnections on the time delay of VLSI circuits," *IEEE Trans. Electron Dev.*, vol. ED-29, pp. 645-650, Mar.1982.

[4] R. Arrathoon (ed.), *Optical Computing: Digital and Symbolic.* New York: Marcel Dekker, Inc., 1989.

[5] "Massively parallel optical-to-electronic data transfer," A research proposal submitted to Army Research Office by Georgia Institute of Technology. Atlanta, GA 30332, Apr. 1988.

[6] A. D. McAulay, "Parallel arrays or vector machines, which direction in VLSI?," *IEEE International Workshop on Computer Systems Organization,* pp. 179-184, 1983.

[7] M. J. Quinn, *Designing Efficient Algorithms for Parallel Computers,* New York: McGraw-Hill, 1987.

[8] M. Eshaghian, H. Jeon, and V. K. Prasanna-Kumar, "Massively parallel architectures with optical interconnection networks," *Proc. SPIE,* vol. 963, pp. 695-702, 1988.

[9] J. W. Goodman, F. Leonberger, S. Kung, and R. Athale, "Optical interconnections for VLSI systems," *Proc. IEEE,* vol. 72, pp. 850-866, July 1984.

[10] H. Winston, *Artificial Intelligence.* Reading, MA: Addison-Wesley, 1984.

[11] E. Charniak and D. McDermott, *Introduction to Artificial Intelligence.* Reading, MA: Addison-Wesley, 1985.

[12] E. Rich, *Artificial Intelligence.* New York: McGraw-Hill, 1983.

[13] S. H. Lee, "Optical analog solutions of partial differential and integral equations," *Opt. Engr.*, vol. 63, pp. 41-47, Jan./Feb. 1985.

[14] A. A. Sawchuk and T. C. Strand, "Digital optical computing," *Proc. IEEE,* vol. 72, pp. 758-779, July 1984.

[15] R. Schmidt and W. T. Cathey, "Optical representations for symbolic logic," *Opt. Engr.*, vol. 27, pp. 475-481, June 1988.

[16] A. Husain, "Optical interconnect of digital integrated circuits and systems," *Proc. SPIE*, vol. 466, pp. 10-20, 1984.

[17] "The MOSIS system (what is it and how to use it)," Report No. ISI/TM-84-128, Univ. of Southern California Information Sciences Institute. Maria Del Rey, CA 90292, Mar. 1984.

[18] J. W. Goodman, A. R. Dias, and L. M. Woody, " Fully parallel, high-speed incoherent optical method for performing discrete Fourier transforms," *Opt. Lett.*, vol 2, pp. 1-3, Jan. 1978.

[19] S. H. Lee and S. C. Esener, "Justifications for a hybrid approach to optical computing," *Proc. SPIE*, vol. 881, pp. 177-178, 1988.

[20] B. Clymer and J. Goodman, "Optical clock distribution to silicon chips," *Opt. Engr.*, vol. 25, pp. 1103-1108, Oct. 1986.

[21] K. Saraswat and F. Mohammadi, "Effect of scaling of interconnections on time delay of VLSI circuits," *IEEE Trans. Electron Dev.*, vol. ED-29, pp. 645-650, Mar. 1982.

[22] L. Bergman, W. Wu, A. Johnston, R. Nixon, S. Esener, G. Guest, P. Yu, T. Drabik, M. Feldman, and S. Lee, "Holographic optical interconnects for VLSI," *Opt. Engr.*, vol. 25, pp. 1109-1118, Oct. 1986.

[23] H. Chou and M. Franklin, "Optical distribution of clock signals in wafer scale digital circuits," in *Proc. 1987 Intnl. Conf. Computer Design.* New York: IEEE, 1987, pp. 117-122.

[24] R. Ade, E. Harstead, A. Amirfazli, T. Cacouris, E. Fossum, P. Prucnal, and R. Osgood, "Silicon photodetector structure for direct coupling of optical fibers to integrated circuits," *IEEE Trans. Electron Dev.*, vol. ED-34, pp. 1283-1289, June 1987.

[25] J. Boyd, R. Wu, D. Zelmon, A. Naumaan, H. Timlin, and H. Jackson, "Guided wave optical structures utilizing silicon," *Opt. Engr.*, vol. 24, pp. 230-234, Apr. 1985.

[26] R. Kostuk, J. Goodman, and L. Hesselink, "Optical imaging applied to microelectronic chip-to-chip interconnections," *Appl. Opt.*, vol. 24, pp. 2851-2858, Sept. 1985.

[27] R. Kostuk, J. Goodman, and L. Hesselink, "Design considerations for holographic optical interconnects," *Appl. Opt.*, vol. 26, pp. 3947-3953, Sept. 1987.

[28] L. Bergman, A. Johnston, R. Nixon, S. Esener, C. Guest, P. Yu, T. Drabik, M. Feldman, and S.H. Lee, "Applications and design considerations for optical interconnects in VLSI," *Proc. SPIE*, vol. 625, pp. 117-126, 1986.

[29] M. Feldman and C. Guest, "Computer generated holographic optical elements for optical interconnection of very large scale integrated circuits," *Appl. Opt.*, vol. 26, pp. 4377-4384, Oct. 1987.

[30] H. Hwang and F. A. Briggs, *Computer Architecture and Parallel Processing*. New York: McGraw-Hill, 1984.

[31] J. Lohstroh, E. Seevinck, and J. de Groot, "Worst-case static noise margin criteria for logic circuits and their mathematical equivalence," *IEEE J. Solid-State Circuits*, vol. SC-18, pp. 803-806, Dec. 1983.

[32] K. Anami, M. Yoshimoto, H. Shinohara, Y. Hirata, and T. Nakano, "Design consideration of a ststic memory cell," *IEEE J. Solid-State Circuits*, vol. SC-18, pp. 414-417, Aug. 1983.

[33] B. Chappel, S. Schuster, and G. Sai-Halasz, "Stability and SER Analysis of Static RAM Cells," *IEEE J. Solid-State Circuits*, vol. SC-20, pp. 383-390, Feb. 1985.

[34] M. R. Ackermann, R. E. Mikawa, L. W. Massengill, and S. E. Diehl, "Factors contributing to CMOS static RAM upset," *IEEE Trans. Nuclear Science*, vol. NS-33, pp. 1524-1529, Dec. 1986.

[35] E. Seevinck, F. List, and J. Lohstroh, "Static-noise margin analysis of MOS SRAM cells," *IEEE J. Solid-State Circuits*, vol. SC-22, pp. 748-754, Oct. 1987.

[36] M. Buehler and R. Allen, "An analytical method for predicting CMOS SRAM upsets with application to asymmetrical memory cells," *IEEE Trans. Nuclear Science*, vol. NS-33, pp. 1637-1641, Dec. 1986.

[37] R. C. Jeager and R. M. Fox, "Phase plane analysis of the upset characteristics of CMOS RAM cells," *Proc. University, Government, and Indistry Microelectronics. Symp.*, pp. 183-187, June 1985.

[38] T. Kacprzak and A. Albicki, "Analysis of metastable operation in RS CMOS flip-flops," *IEEE J. Solid-State Circuits*, vol. SC-22, pp. 57-63, Feb. 1987.

[39] W. Wu and A. R. Johnston, "CMOS detector cells for holographic optical interconnects in microcircuits," *Proc. SPIE*, vol. 752, pp. 192-199, 1987.

[40] W. Wu, L. A. Bergman, R. A. Allen, and A. R. Johnston, "Optical addressing techniques for a CMOS RAM," *Proc. SPIE*, vol. 836, pp. 351-358, 1987.

[41] M. J. Murdocca and B. Sugla, "Design for an optical random access memory," *Appl. Opt.*, vol. 28, pp.182-188, Jan. 1989.

[42] H. J. M. Veendrick, "The behavior of flip-flops used as synchronizers and prediction of their failure rate," *IEEE J. Solid-State Circuits*, vol. SC-15, pp. 169-176, Apr. 1980.

[43] A. Mukerjee, *Introduction to nMOS and CMOS VLSI System Design*. Englewood Cliffs, NJ: Prentice-Hall, 1986.

[44] L. A. Glasser and D. W. Dobberpuhl, *The Design and Analysis of VLSI Circuits.* Reading, MA: Addison-Wesley, 1985.

[45] H. Okuyama, T. Nakano, S. Nishida, E. Aono, H. Satoh, and S. Arita, "A 7.5-ns 32K x 8 CMOS SRAM," *IEEE J. Solid-State Circuits,* vol. SC-23, pp. 1054-1059, Oct. 1988.

[46] Y. Kohno, T. Wada, K. Anami, Y. Kawai, K. Yuzuriha, T. Matsuhawa, and S. Kayano, "A 14-ns 1-Mbit CMOS SRAM with variable bit organization," *IEEE J. Solid-State Circuits,* vol. SC-23, pp. 1060-1066, Oct. 1988.

[47] D. Wong, R. Adams, A. Bhattacharyya, J. Covino, J. Gabric, and G. Lattimore, "An 11-ns 8K x 18 CMOS static RAM with 0.5-μm devices," *IEEE J. Solid-State Circuits,* vol. SC-23, pp. 1095-1103, Oct. 1988.

[48] K. Sasaki, S. Hanamura, K. Veda, T. Oono, O. Minato, Y. Sakai, S. Meguro, M. Tsunematsu, T. Masuhara, M. Kubotera, and H. Toyoshima, "A 15-ns 1-Mbit CMOS SRAM,"*IEEE J. Solid-State Circuits,* vol. SC-23, pp. 1067-1072, Oct. 1988.

[49] T. O'Connell, J. Hartman, E. Errett, G. Leach, and W. Dunn, "A 4K static clocked and nonclocked RAM design," *Proc. 1977 IEEE Intnl. Solid-State Circuits Conf.,* pp. 14-15, 1977.

[50] S. T. Flannagan, "Synchronization reliability in CMOS technology," *IEEE J. Solid-State Circuits,* vol. SC-20, pp. 880-882, Aug. 1985.

[51] J. Uyemura, *Fundamentals of MOS Digital Integrated Circuits.* Reading, MA: Addison-Wesley, 1988.

[52] J. C. Pickel and J. T. Blandford, "Cosmic ray induced errors in MOS memory cells," *IEEE Trans. Nuclear Science,* vol. NS-26, pp. 1166-1167, Dec. 1978.

[53] S. M. Sze, *Physics of Semiconductor Devices.* New York: Wiley-Interscience, 1981.

[54] H. Beneking, "Gain and bandwidth of fast near-infrared photodetectors: A comparison of diodes, phototransistors, and photoconductive devices," *IEEE Trans. Electron Dev.,* vol. ED-29, pp. 1420-1431, Sept. 1982.

[55] G. Anderson, B. Guenther, J. Hynecek, J. Keys, and A. Vanderlugt, "Role of photodetectors in optical signal processing," *Appl. Opt.,* vol. 27, pp. 2871-2886, July 1988.

[56] J. Palmer, "Near-infrared limitations to silicon photodetection self-calibration," *Proc. SPIE,* vol. 499, pp. 7-14, 1984.

[57] A. Yariv, *Optical Electronics.* New York: Holt, Rinehart and Winston, 1985, pp. 367-380.

[58] B. Culshaw, "Photodetectors and photodetection," *Sensors and Actuators*, vol. 10, pp. 263-285, Oct. 1986.

[59] E. Dereniak and D. Crowe, *Optical Radiation Detectors*. New York: John Wiley and Sons, 1984, ch.3.

[60] O. Christensen, "Quantum efficiency of the internal photoelectric effect in silicon and germanium," *J. Appl. Phys.*, vol. 47, pp. 689-695, Feb. 1976.

[61] E. Yang, *Fundamentals of Semiconductor Devices*. New York: McGraw-Hill, 1978, pp. 27-28.

[62] P. Witherell and M. Faulhaber, "The silicon solar cell as a photometric detector," *Appl. Opt.*, vol. 9, pp. 73-78, Jan. 1970.

[63] K. L. Su, *Fundamentals of Circuits, Electronics, and Signal Analysis*. Boston: Houghton Mifflin, 1978, ch. 6.

[64] D. J. Comer, *Modern Electronic Circuit Design*. Reading, MA: Addison-Wesley, 1978, ch. 8.

[65] J. R. Meyer-Arendt, *Introduction to Classical and Modern Optics*. Englewood Cliffs, NJ: Princeton-Hall, pp. 272-275, 1984.

[66] E. S. Yang, *Microelectronic Devices*. New York: McGraw-Hill,1988, pp. 368-370.

[67] W. Shockley, *Electrons and Holes in Semiconductors*. Princeton, NJ: Van Nostrand, 1950.

[68] K. Brennan, "Semiconductor Device Physics," published notes, Georgia Institute of Technology, 1988.

[69] P. Allen and D. Holberg, *CMOS Analog Circuit Design*. New York: Holt, Rinehart and Winston, 1987.

[70] R. Geiger, P. Allen, and N. Strader, *VLSI Design Techniques for Analog and Digital Circuits*. New York: McGraw-Hill, 1989.

[71] J. Tanida and Y. Ichioka, "Optical logic array processor using shadow-grams," *J. Opt. Soc. Amer.*, vol. 73, pp. 800-809, June 1983.

[72] Y. Ichioka and J. Tanida, "Optical parallel logic gates using a shadow-casting system for optical digital computing," *Proc. IEEE*, vol. 72, pp. 787-801, July 1984.

[73] D. Feitelson, *Optical Computing: A Survey for Computer Scientists*. London: The MIT Press,1988.

[74] K-H Brenner, "New implementation of symbolic logic," *Appl. Opt.*, vol. 25, pp. 3061-3064, Sep. 1986.

[75] M. J. Murdocca, "Digital optical computing with one-rule cellular automata," *Appl. Opt.*, vol. 26, pp. 682-688, Feb. 1987.

[76] S. L. Hurst, "Multiple valued logic-its status and its future," *IEEE Trans. Computers*, vol. C-33, pp. 1160-1179, Dec. 1984.

[77] A. Yariv, S-K. Kwong, and K. Kyuma, "Demonstration of an all-optical accosiative holographic memory," *Appl. Phys. Lett.*, vol. 48, pp. 1114-1116, Apr. 1986.

[78] N. Matloff, S. Kowel, and C. Eldering, "OPTIMUL: An optical interconnect for multiprocessor systems," *International Conference on Supercomputing*, vol. 100, pp. 16-24, 1988.

VITA

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